

Revision : 1.01

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24	AUDIO JACK
25	FAN/HWMO KB/MS

[illegible]

			
Title			
COVER SHEET			
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Model Name:GA-970A-UD3P

Component value change history

Version: 1.01

4 Layer, 4mil 50ohm +/- 15% L

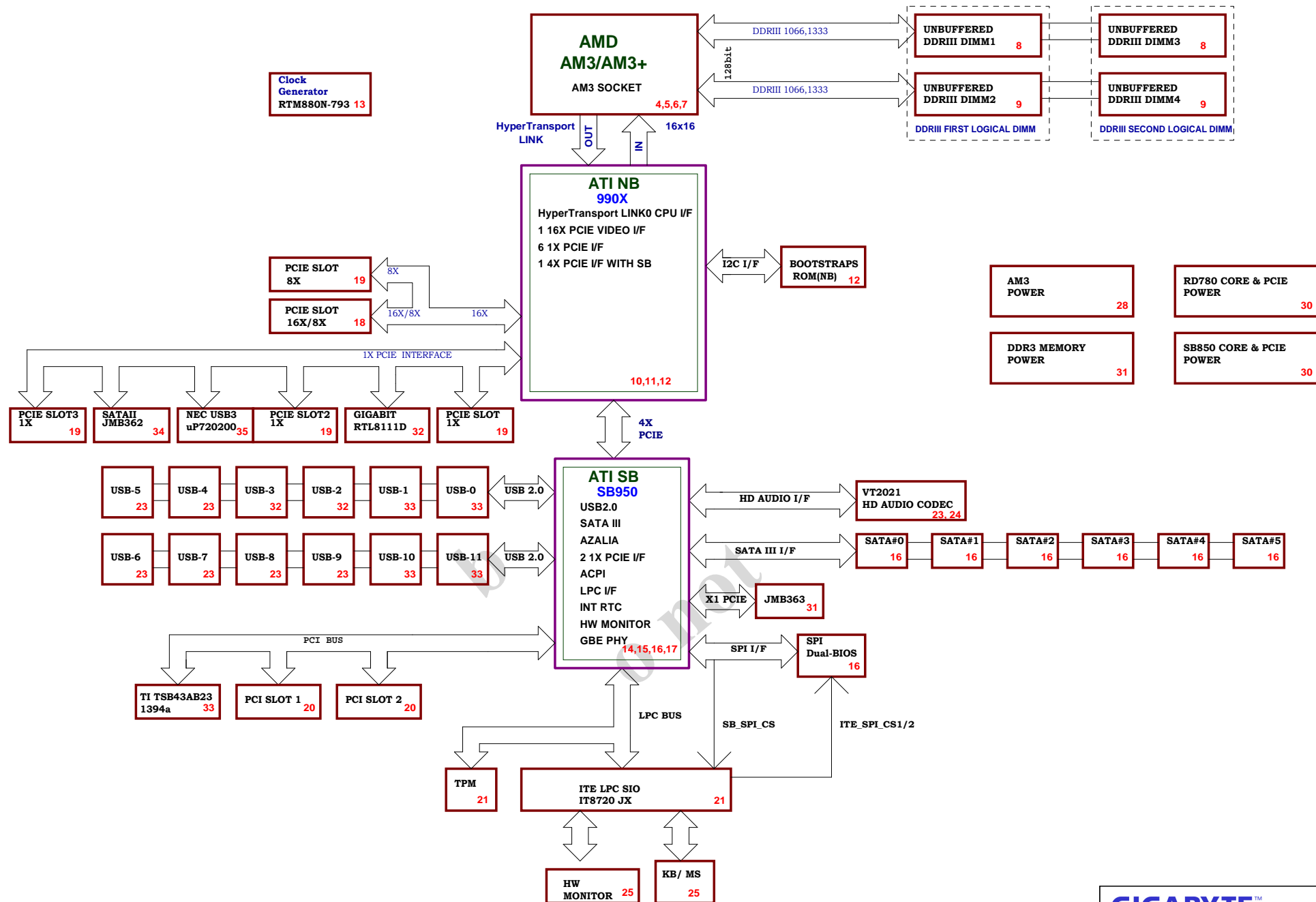
P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

[illegible]

GIGABYTE™			
Title			
BOM & PCB HISTORY			
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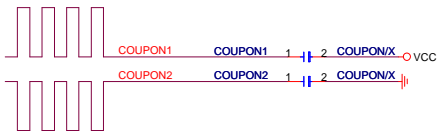
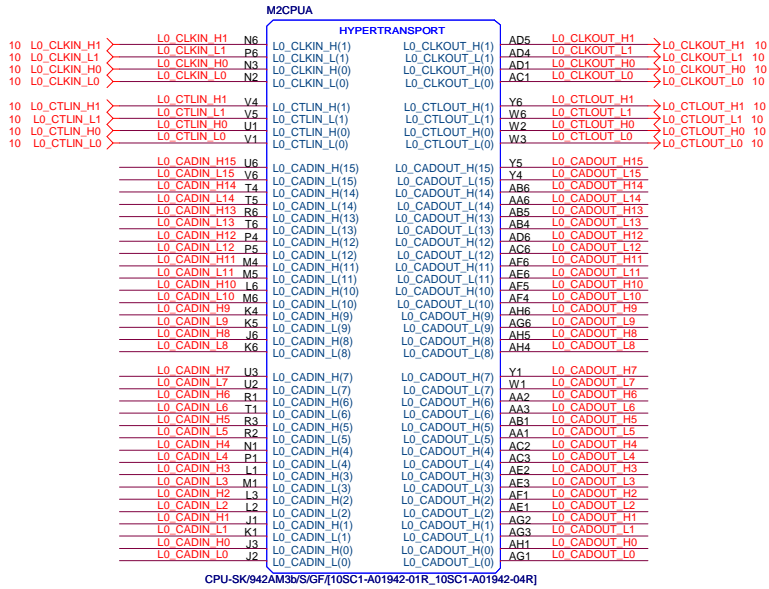
www.schematic-x.blogspot.com

GIGABYTE™			
BLOCK DIAGRAM			
Title	Document Number	Rev	
Size	Custom	GA-970A-UD3P	1.01
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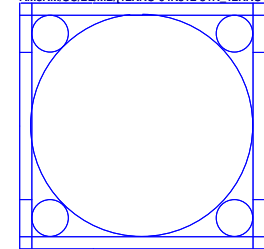
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

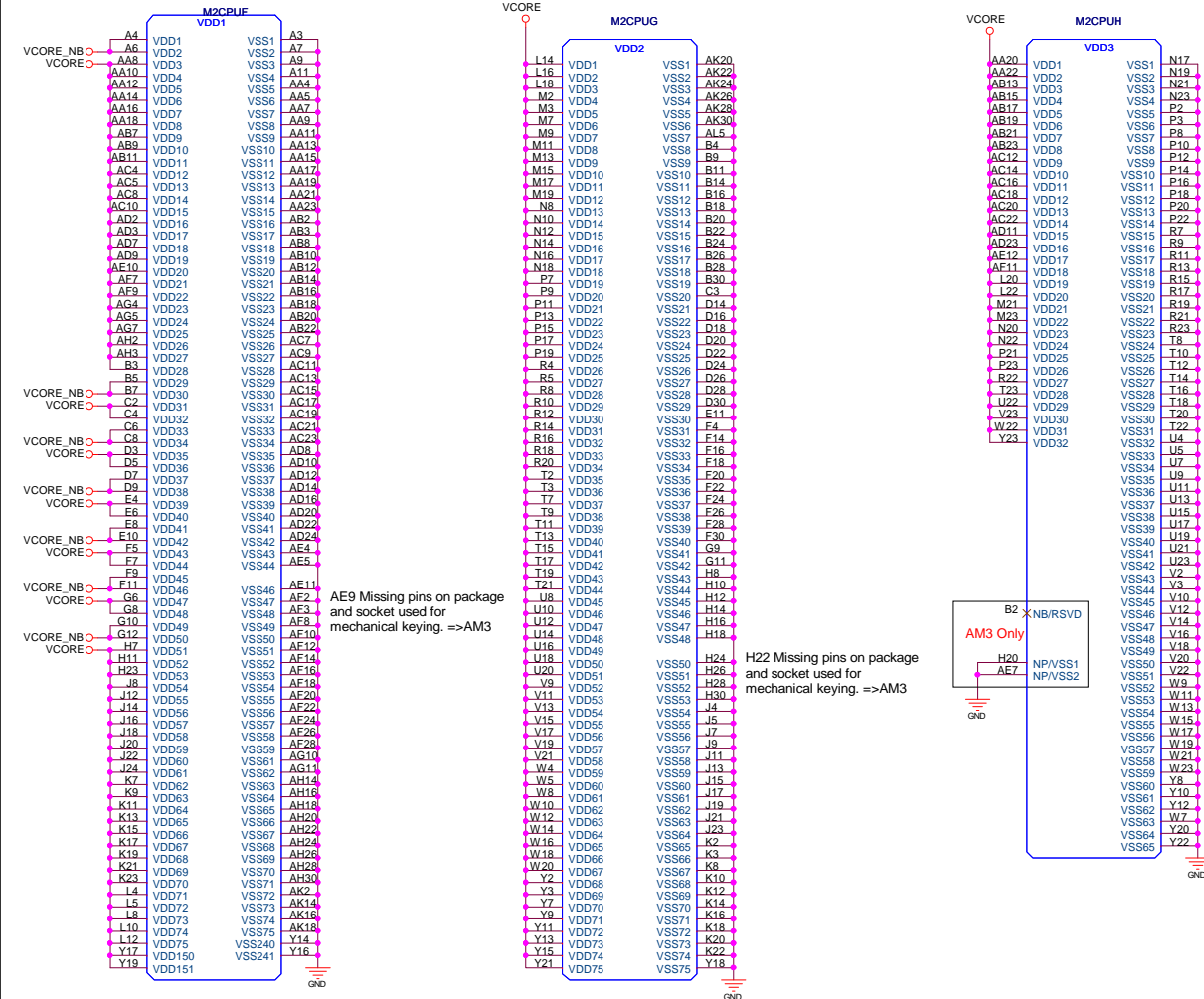


M2CPU
AM3RM/SC/BL/MB/12KRC-04K812-31R_12KRC-04K812-32R



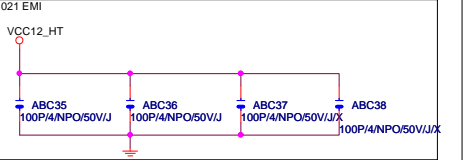
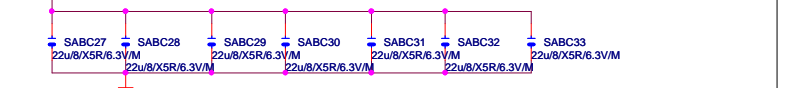
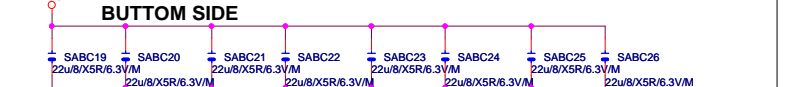
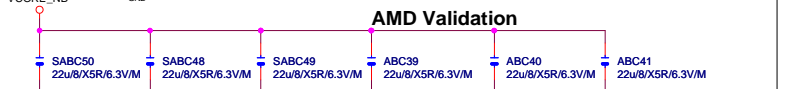
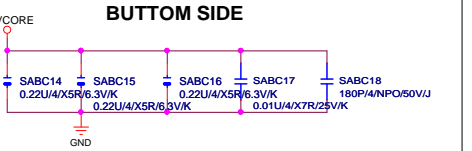
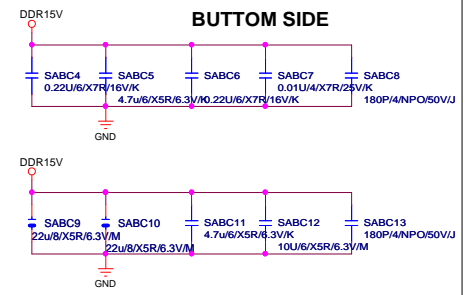
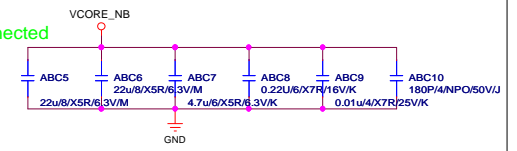
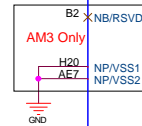
GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
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VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

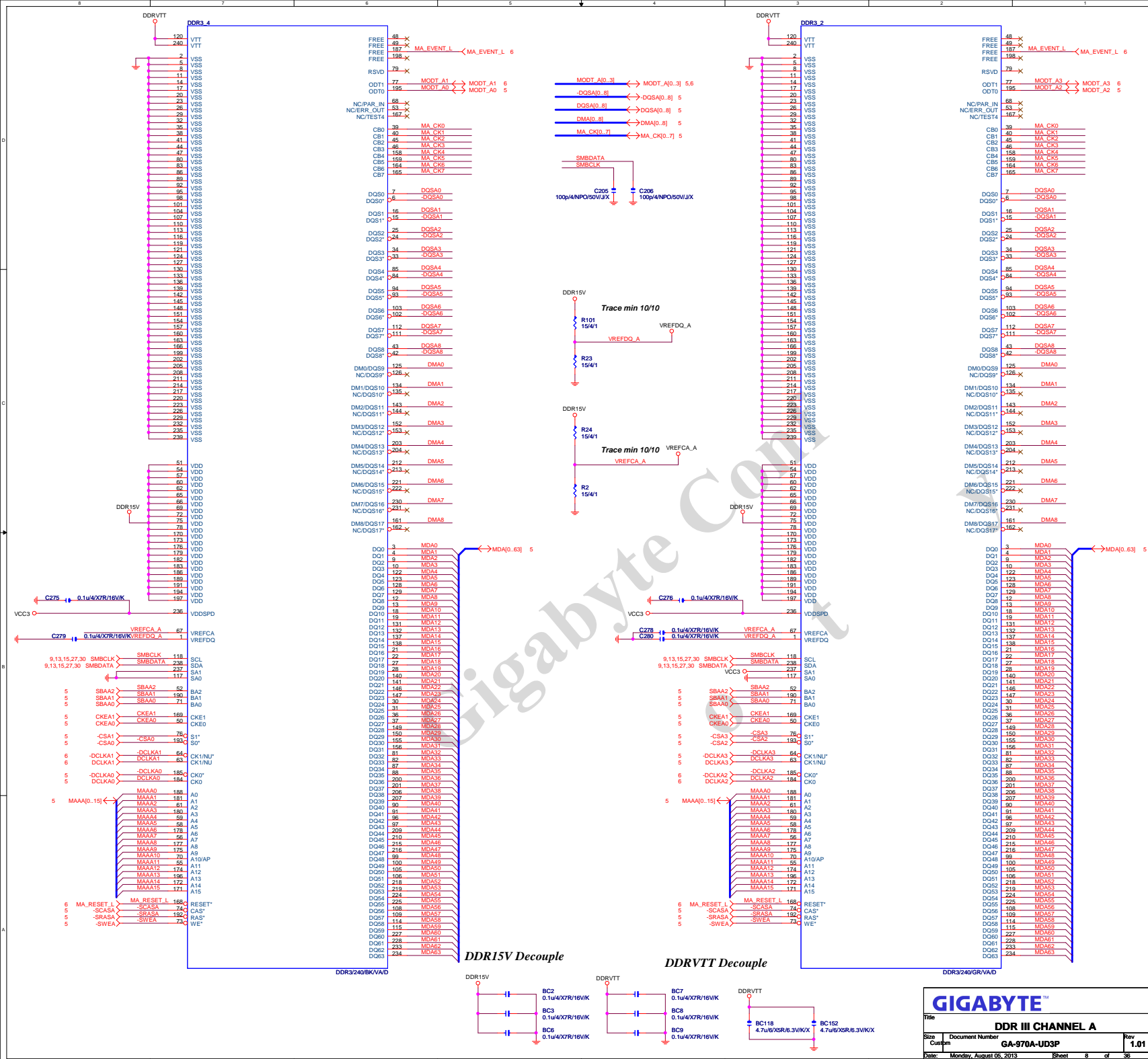


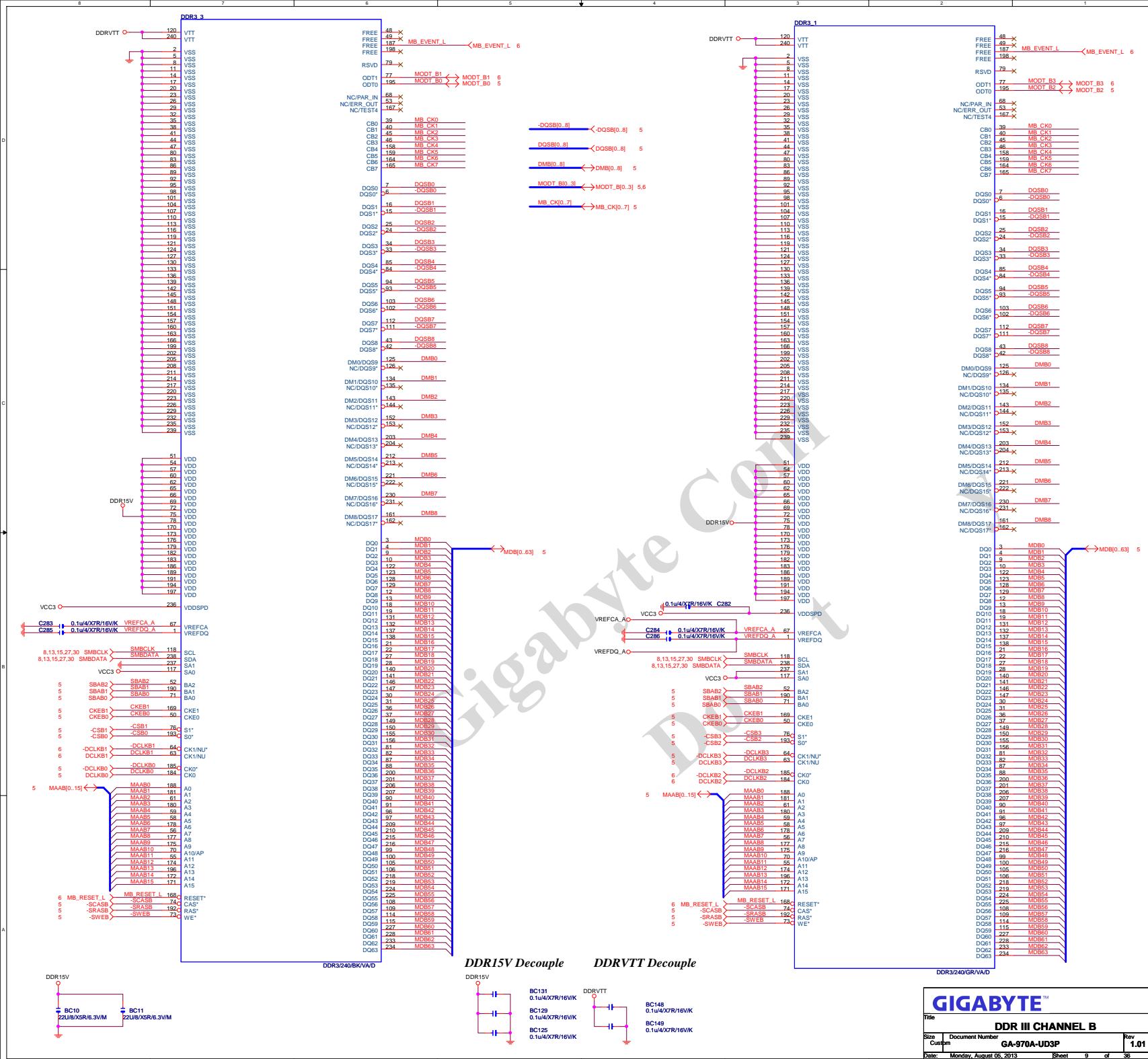
AE9 Missing pins on package and socket used for mechanical keying. =>AM3

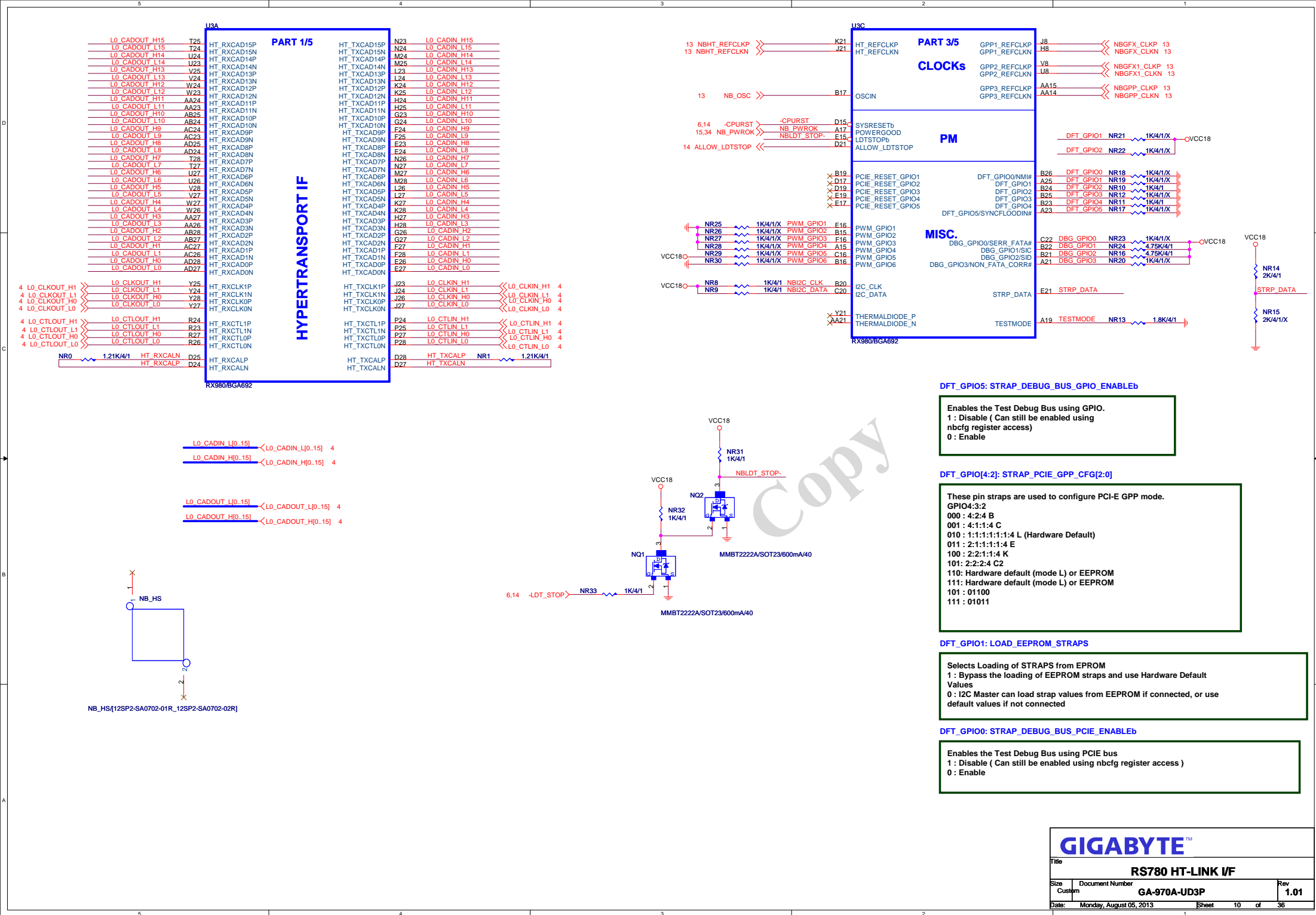
H22 Missing pins on package and socket used for mechanical keying. =>AM3



GIGABYTE™			
CPU POWER & GND			
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PART 2/5			
EXP A_RXP15	N6	GPP1_RX15P	N3
EXP A_RXN15	N5	GPP1_RX15N	N2
EXP A_RXP14	M5	GPP1_RX14P	M1
EXP A_RXN14	M4	GPP1_RX14N	M2
EXP A_RXP13	L6	GPP1_RX13P	L3
EXP A_RXN13	L5	GPP1_RX13N	L2
EXP A_RXP12	K5	GPP1_RX12P	K2
EXP A_RXN12	K4	GPP1_RX12N	K1
EXP A_RXP11	J6	GPP1_RX11P	J3
EXP A_RXN11	J5	GPP1_RX11N	J2
EXP A_RXP10	H5	GPP1_RX10P	H2
EXP A_RXN10	H4	GPP1_RX10N	H1
EXP A_RXP9	G6	GPP1_RX9P	G3
EXP A_RXN9	G5	GPP1_RX9N	G2
EXP A_RXP8	F5	GPP1_RX8P	F2
EXP A_RXN8	F4	GPP1_RX8N	F1
EXP A_RXP7	D2	GPP1_RX7P	E3
EXP A_RXN7	D1	GPP1_RX7N	E2
EXP A_RXP6	B5	GPP1_RX6P	A4
EXP A_RXN6	C5	GPP1_RX6N	B4
EXP A_RXP5	D6	GPP1_RX5P	A6
EXP A_RXN5	E6	GPP1_RX5N	B6
EXP A_RXP4	E7	GPP1_RX4P	B7
EXP A_RXN4	F7	GPP1_RX4N	C7
EXP A_RXP3	D8	GPP1_RX3P	A8
EXP A_RXN3	E8	GPP1_RX3N	B8
EXP A_RXP2	E9	GPP1_RX2P	B9
EXP A_RXN2	F9	GPP1_RX2N	C9
EXP A_RXP1	D10	GPP1_RX1P	A10
EXP A_RXN1	E10	GPP1_RX1N	B10
EXP A_RXP0	E11	GPP1_RX0P	B11
EXP A_RXN0	F11	GPP1_RX0N	C11

AC9	GPP2_RX15P	AF9
AD9	GPP2_RX15N	AG9
AE8	GPP2_RX14P	AG8
AE7	GPP2_RX14N	AH8
AC7	GPP2_RX13P	AF7
AD7	GPP2_RX13N	AG7
AD6	GPP2_RX12P	AG6
AE6	GPP2_RX12N	AH6
AE5	GPP2_RX11P	AG4
AG5	GPP2_RX11N	AH4
AF2	GPP2_RX10P	AE3
AD2	GPP2_RX10N	AE2
AD1	GPP2_RX9P	AC3
AB5	GPP2_RX8P	AC2
AB4	GPP2_RX8N	AB2
AA6	GPP2_RX7P	AB1
AA5	GPP2_RX7N	AA3
Y5	GPP2_RX6P	AA2
Y4	GPP2_RX6N	Y2
W6	GPP2_RX5P	Y1
W5	GPP2_RX5N	W3
V5	GPP2_RX4P	W2
V4	GPP2_RX4N	V2
U6	GPP2_RX3P	V1
U5	GPP2_RX3N	U2
T5	GPP2_RX2P	T2
T4	GPP2_RX2N	T1
R6	GPP2_RX1P	R3
R5	GPP2_RX1N	R2
P5	GPP2_RX0P	P2
P4	GPP2_RX0N	P1

AD11	GPP3_RX9P	AH10
AC11	GPP3_RX9N	AG10
AE12	GPP3_RX8P	AG11
AD12	GPP3_RX8N	AE11
AD13	GPP3_RX7P	AH12
AC13	GPP3_RX7N	AG12
AE14	GPP3_RX6P	AE13
AD14	GPP3_RX6N	AH14
AD15	GPP3_RX5P	AG14
AC15	GPP3_RX5N	AG15
AE16	GPP3_RX4P	AE16
AD16	GPP3_RX4N	AE17
AD17	GPP3_RX3P	AG16
AC17	GPP3_RX3N	AG17
AE18	GPP3_RX2P	AE17
AD18	GPP3_RX2N	AH18
AD19	GPP3_RX1P	AG18
AC19	GPP3_RX1N	AG19
AH20	GPP3_RX0P	AF19
AG20	GPP3_RX0N	

AC21	SB_RX3P	AG22
AD21	SB_RX3N	AH22
AE22	SB_RX2P	AE21
AF25	SB_RX2N	AG21
AG25	SB_RX1P	AE23
AG26	SB_RX1N	AG23
AH26	SB_RX0P	NC18
	SB_RX0N	AH24



RX980/BGA692

PCI_E slot TX need CAP close to slot side

NC6	0.1u/4X7R/16V/K	ML_OP
NC5	0.1u/4X7R/16V/K	ML_ON
NC6	0.1u/4X7R/16V/K	GPP_TX3P_C
NC5	0.1u/4X7R/16V/K	GPP_TX3N_C
NC6	0.1u/4X7R/16V/K	GPP_TX2P_C
NC5	0.1u/4X7R/16V/K	GPP_TX2N_C
NC6	0.1u/4X7R/16V/K	GPP_TX1P_C
NC5	0.1u/4X7R/16V/K	GPP_TX1N_C
NC2	0.1u/4X7R/16V/K	USB3_OP
NC1	0.1u/4X7R/16V/K	USB3_ON

NC11	0.1u/4X7R/16V/K	A_TX3P
NC12	0.1u/4X7R/16V/K	A_TX3N
NC14	0.1u/4X7R/16V/K	A_TX2P
NC13	0.1u/4X7R/16V/K	A_TX2N
NC15	0.1u/4X7R/16V/K	A_TX1P
NC16	0.1u/4X7R/16V/K	A_TX1N
NC18	0.1u/4X7R/16V/K	A_TX0P
NC17	0.1u/4X7R/16V/K	A_TX0N

PLACE THESE CAP CLOSE TO NB.

GIGABYTE™

Title
RS780 PCIE I/F ,Switch

Size Document Number
Custom **GA-970A-UD3P**

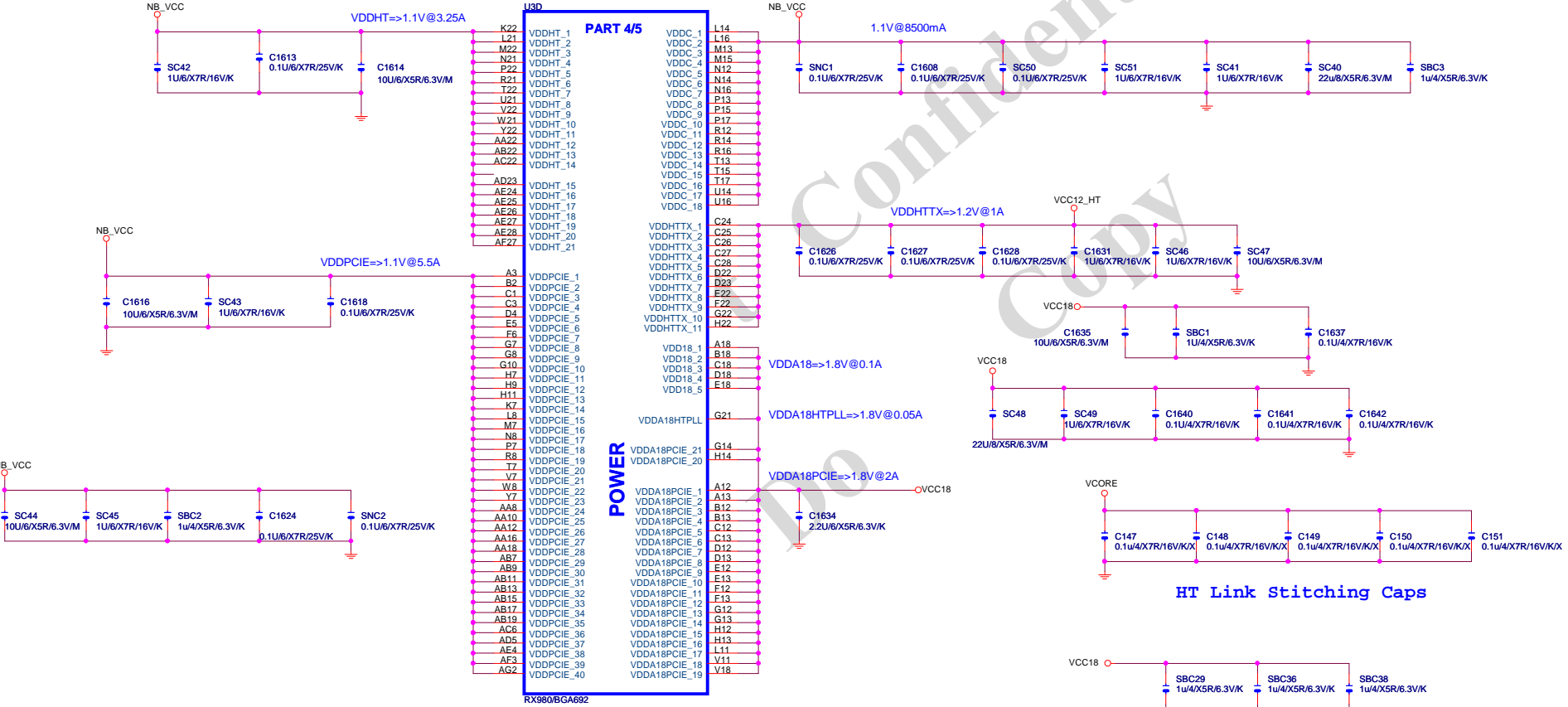
Rev
1.01

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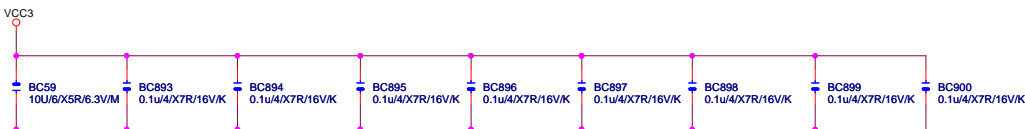
GROUND

VS141 VS142 VS143 VS144 VS145 VS146 VS147 VS148 VS149 VS150 VS151 VS152 VS153 VS154 VS155 VS156 VS157 VS158 VS159 VS160 VS161 VS162 VS163 VS164 VS165 VS166 VS167 VS168 VS169 VS170 VS171 VS172 VS173 VS174 VS175 VS176 VS177 VS178 VS179 VS180 VS181 VS182 VS183 VS184 VS185 VS186 VS187 VS188 VS189 VS190 VS191 VS192 VS193 VS194 VS195 VS196 VS197 VS198 VS199 VS200 VS201 VS202 VS203 VS204 VS205 VS206 VS207 VS208 VS209 VS210 VS211 VS212 VS213 VS214 VS215 VS216 VS217 VS218 VS219 VS220 VS221 VS222 VS223 VS224 VS225 VS226 VS227 VS228 VS229 VS230 VS231 VS232 VS233 VS234 VS235 VS236 VS237 VS238 VS239 VS240 VS241 VS242 VS243 VS244 VS245 VS246 VS247 VS248 VS249 VS250 VS251 VS252 VS253 VS254 VS255 VS256 VS257 VS258 VS259 VS260 VS261

RX980/BGA692

**GIGABYTE**Title
RS780 POWER & GNDSize
Customer Document Number
GA-970A-UD3PRev
1.01

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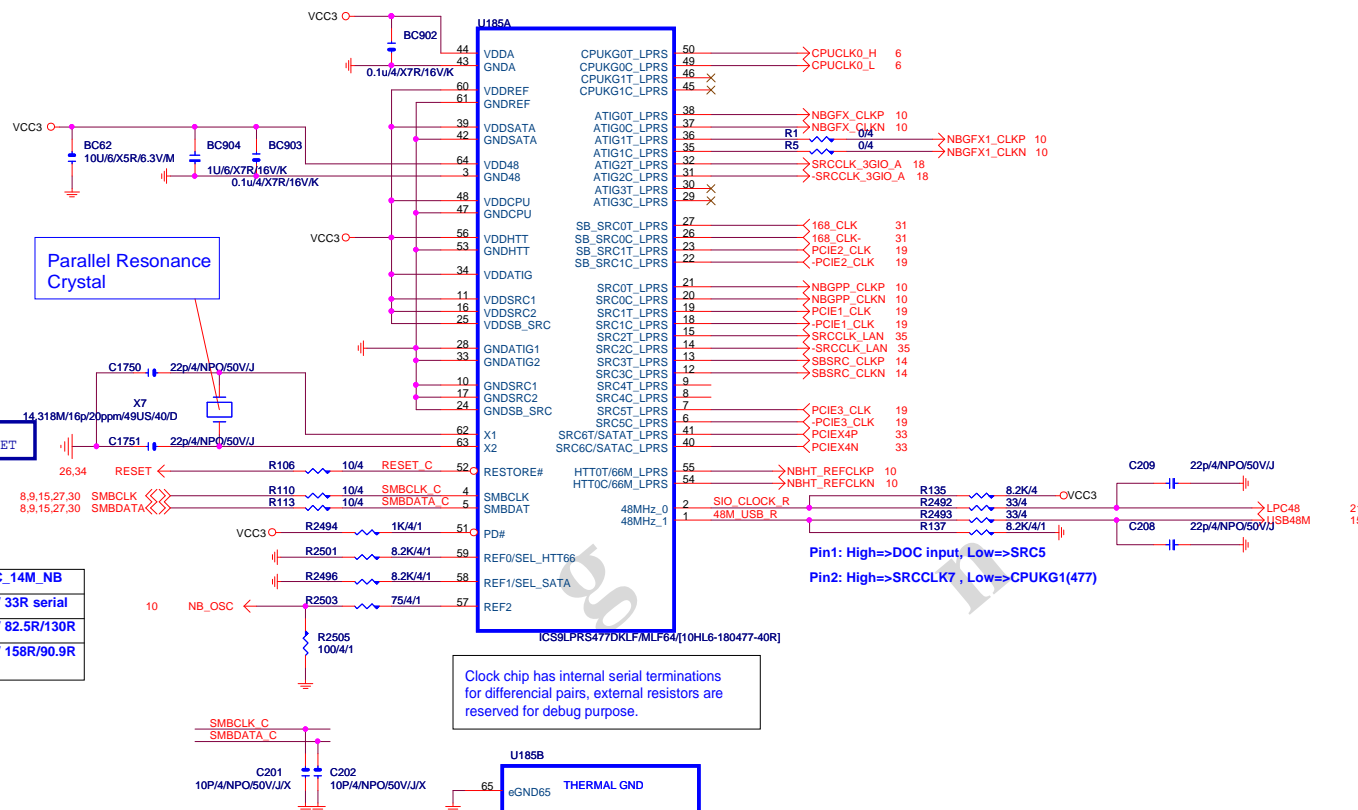
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



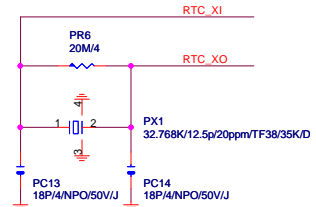
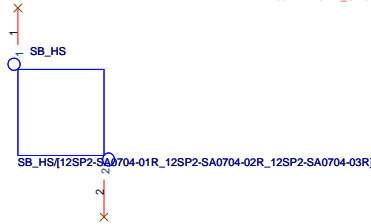
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

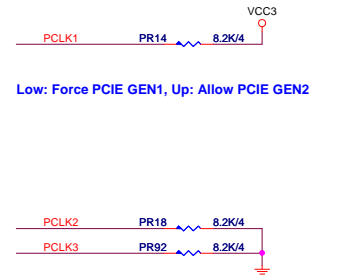
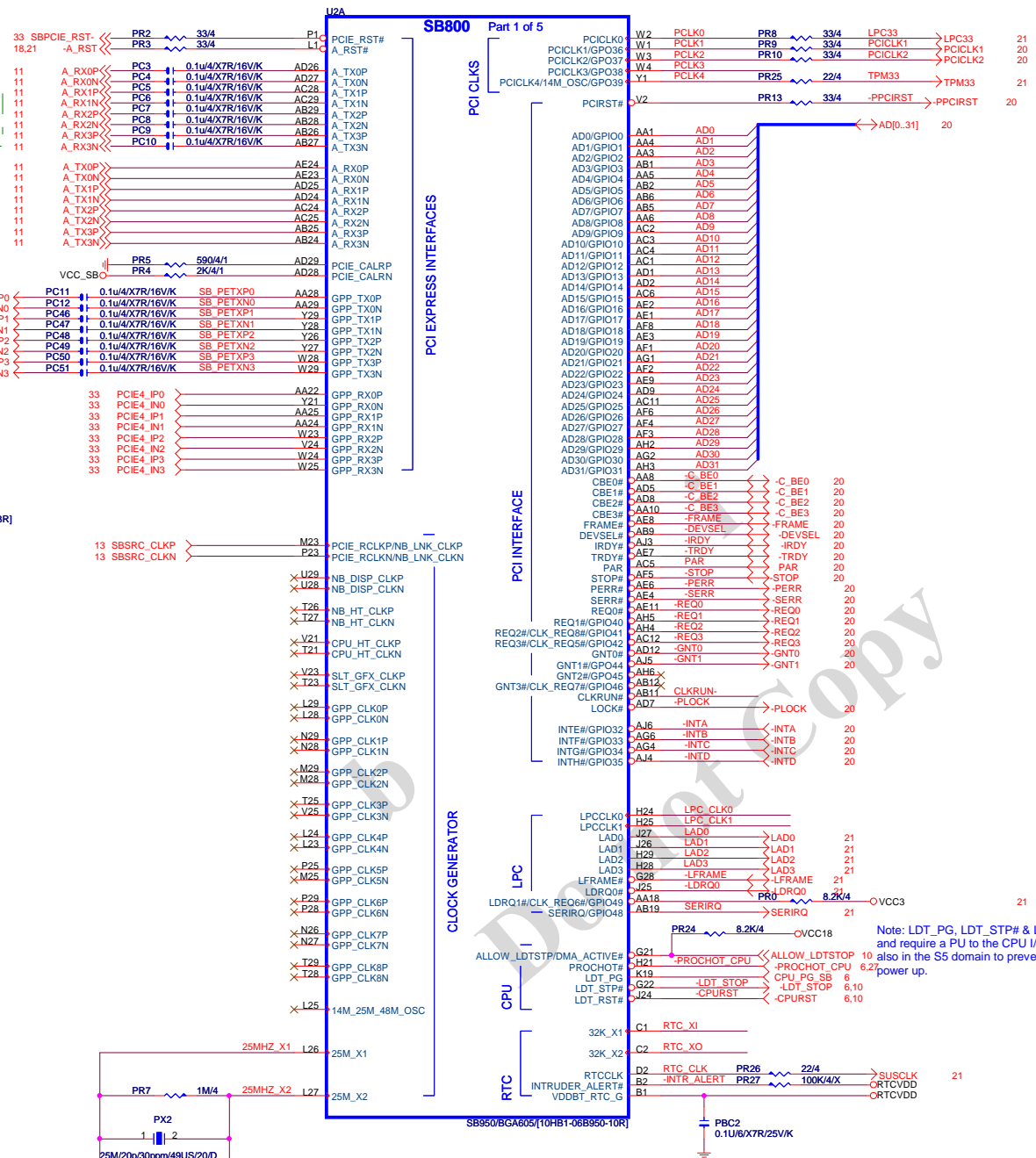
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

S.B HEATSINK

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850



SHW/DO.64*5.08*6.74



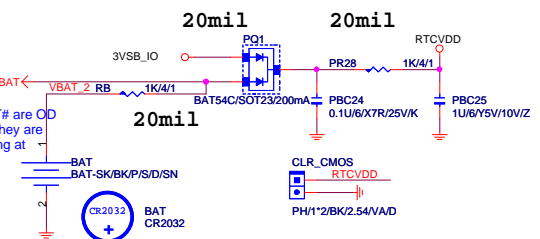
PULL HIGH
WATCHDOG TIMER ON NB_PWRGD ENABLED
PULL LOW
WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT

PULL HIGH
WATCHDOG TIMER ON NB_PWRGD ENABLED
PULL LOW
WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT

BIOS after boot setting
EC AOD-ACC

LPC_CLK0
Rev.A12
PULL HIGH
IMC ENABLED
PULL LOW
IMC DISABLED DEFAULT

LPC_CLK1
CLKGEN
ENABLED
CLKGEN
DISABLED
DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

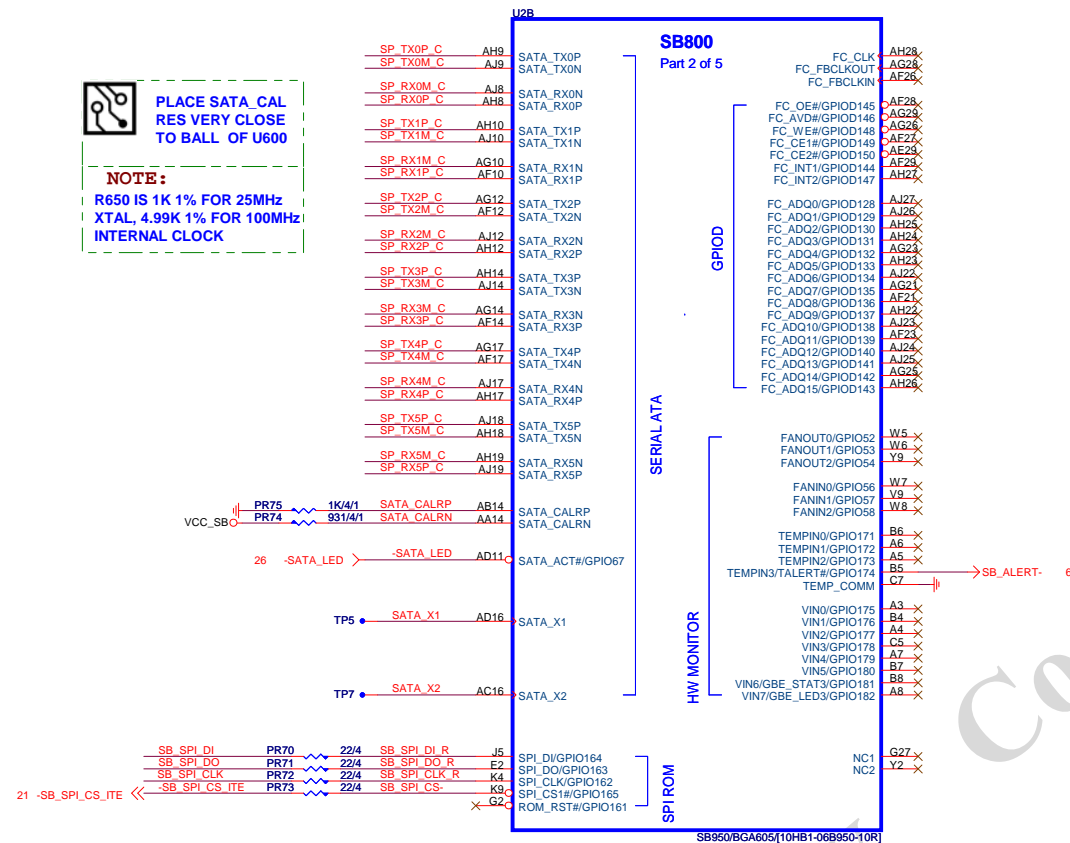
GIGABYTE
Title
ATI SB700 PCIE/PCI/CPU/LPC
Size Custom
Document Number
GA-970A-UD3P
Date: Monday, August 05, 2013
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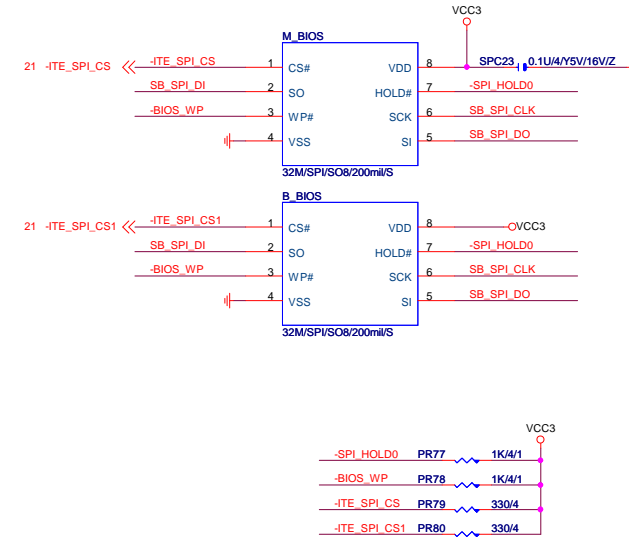
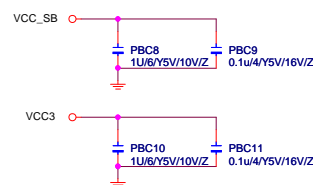
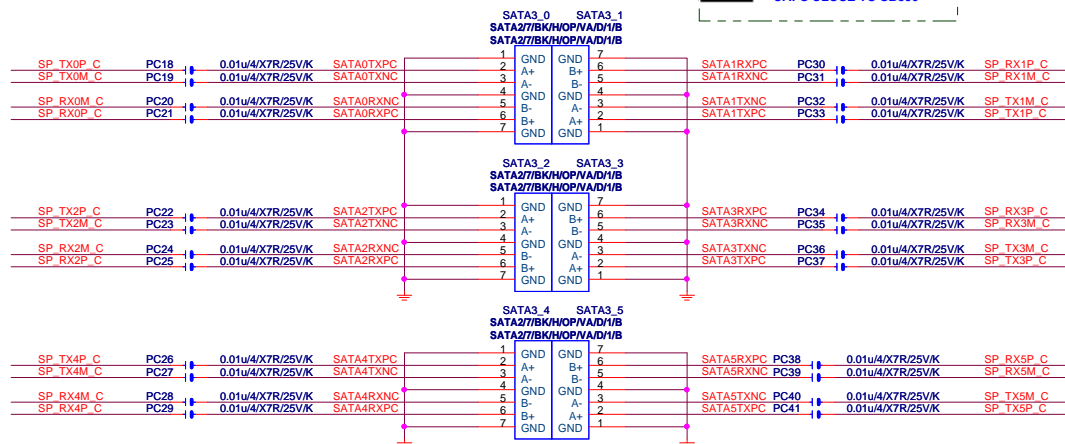
PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

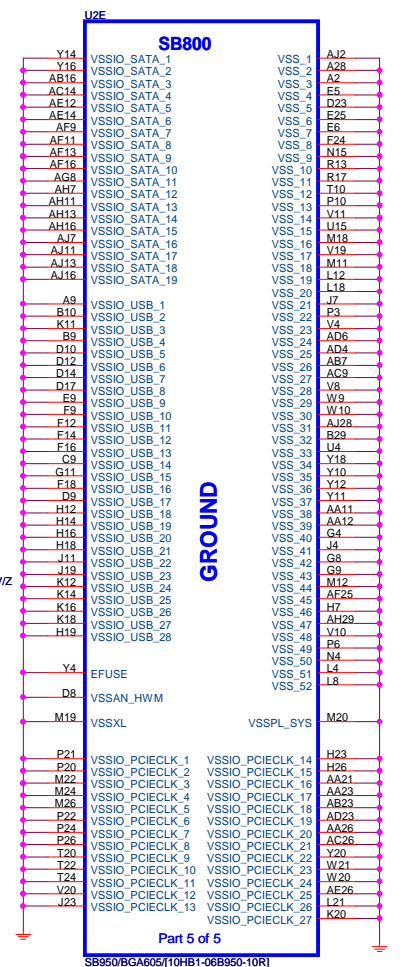


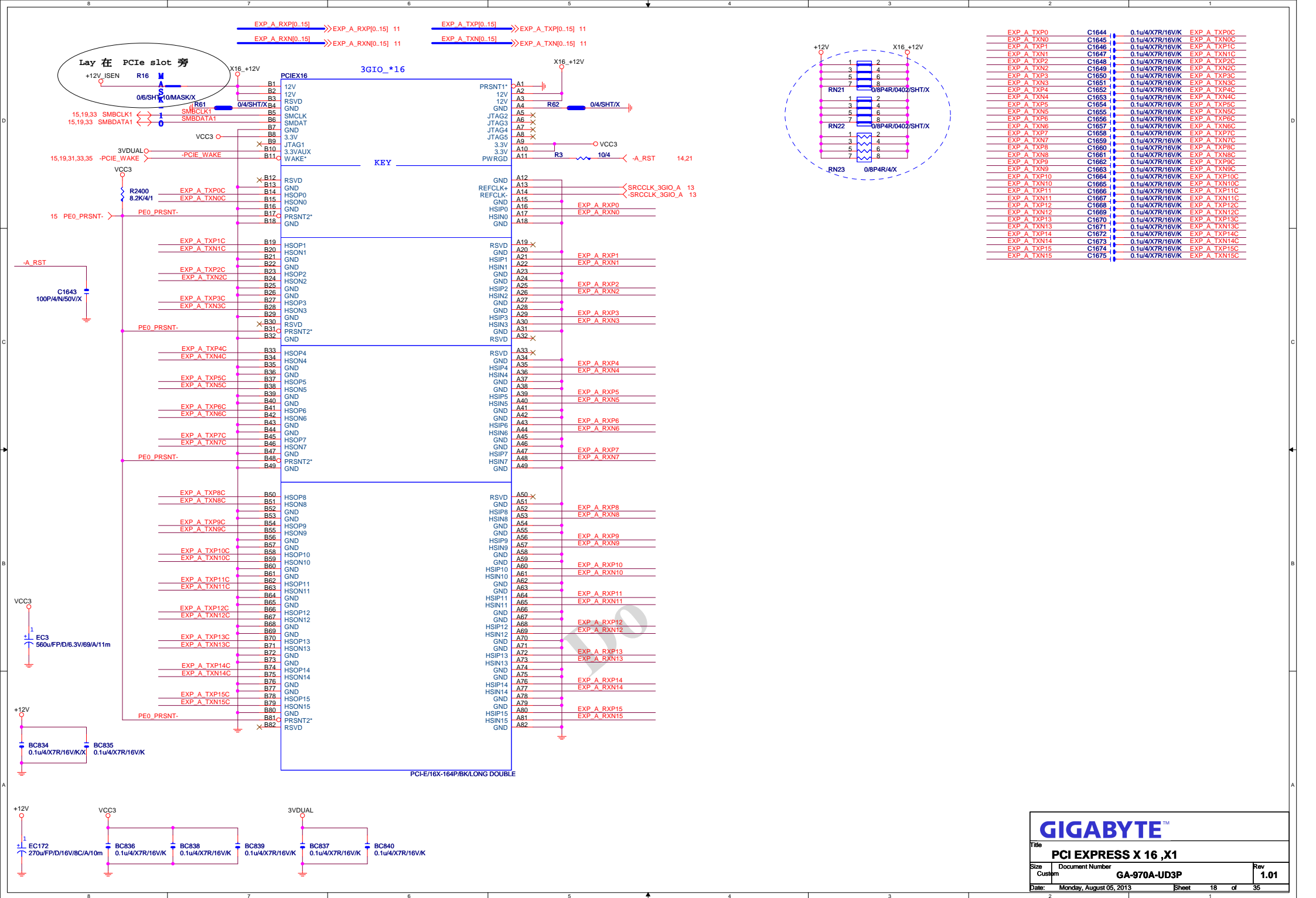
PLACE SATA AC COUPLING
CAPS CLOSE TO SB800

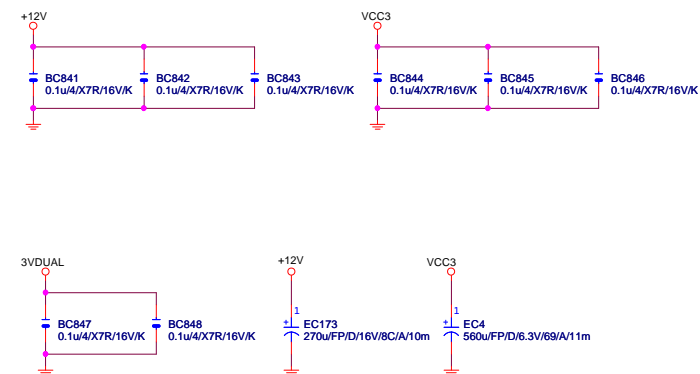
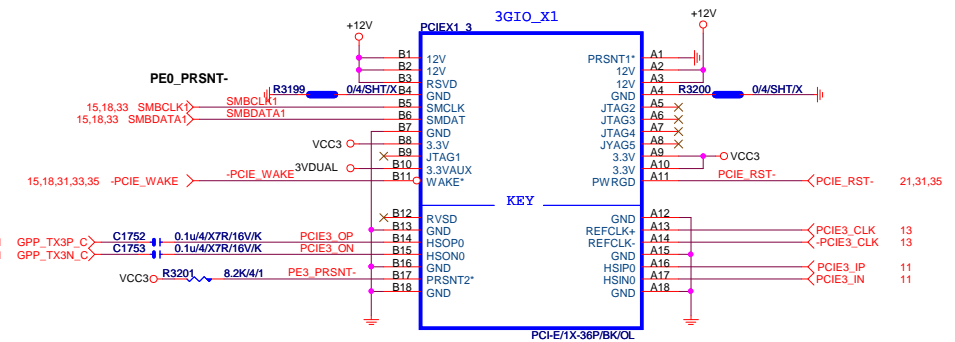


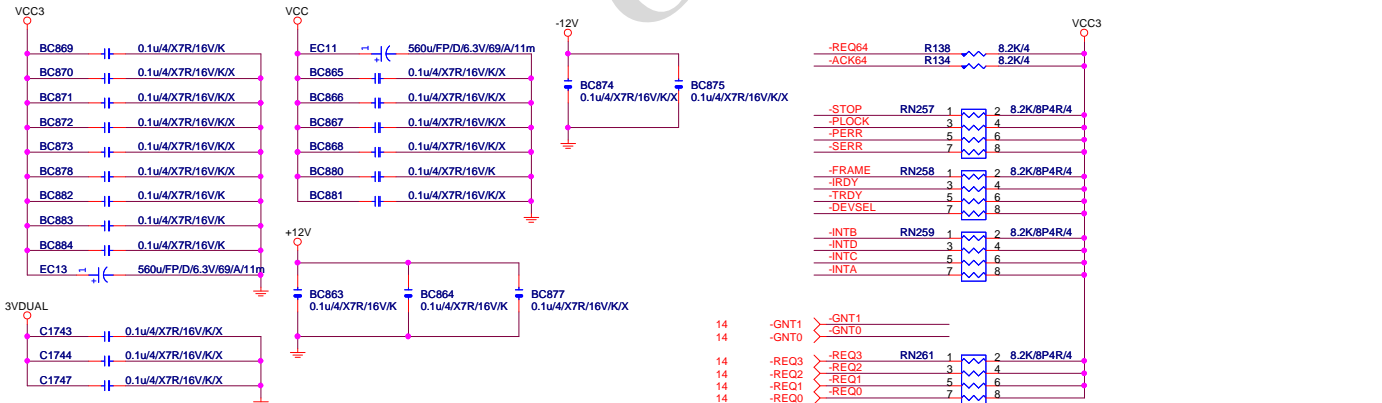
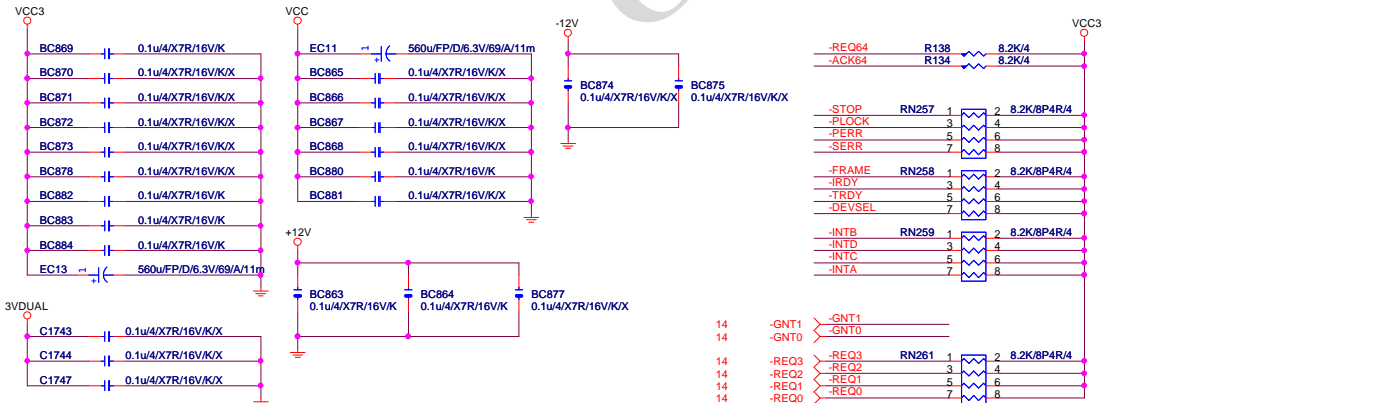
GIGABYTE

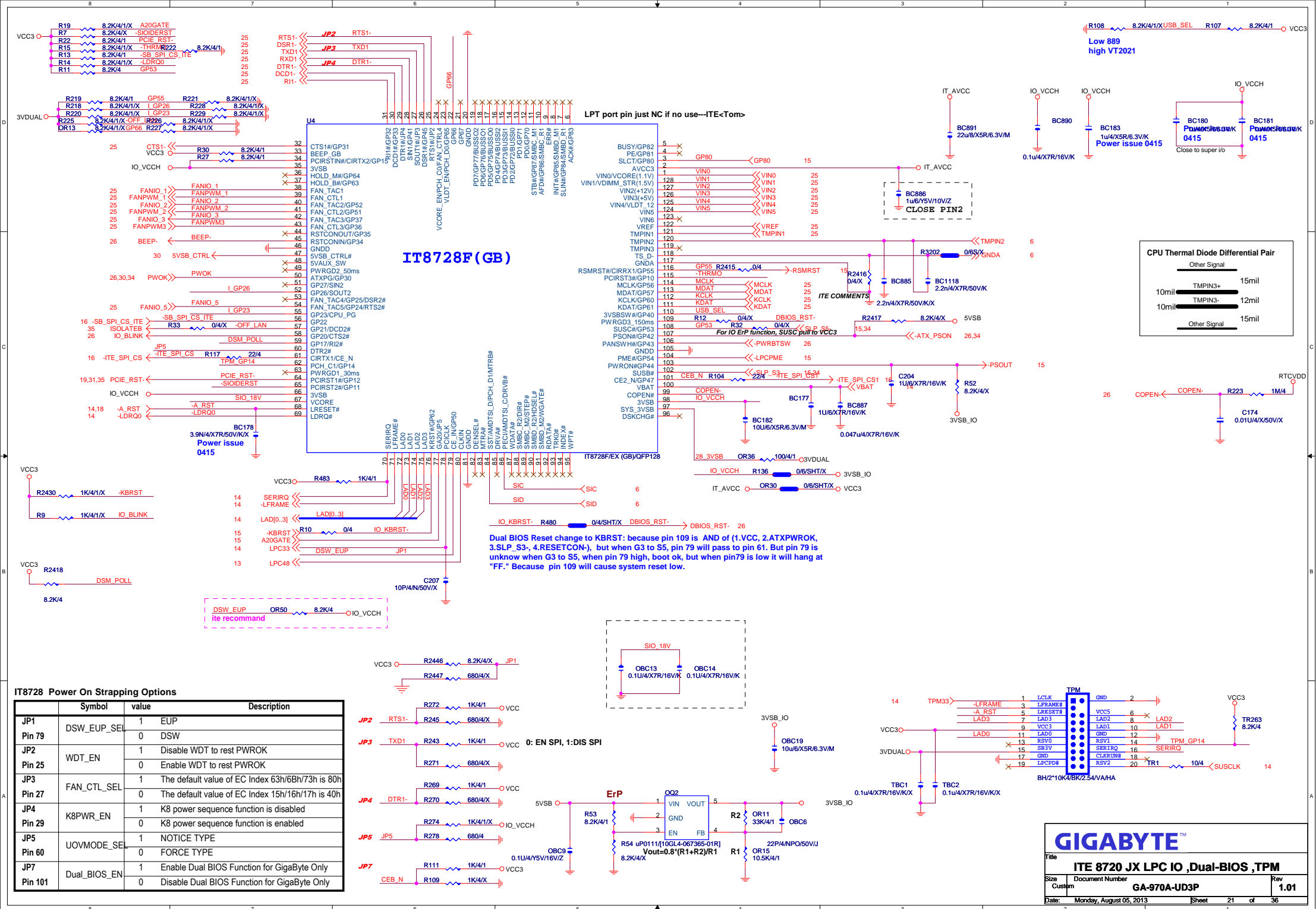
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Size	Document Number	Rev	1.01
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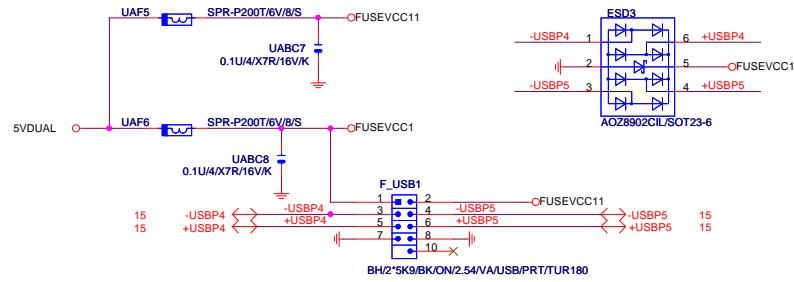




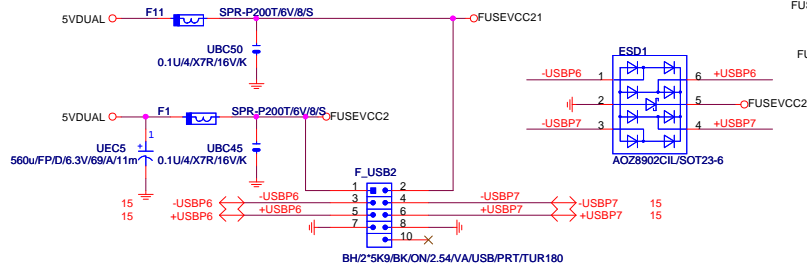




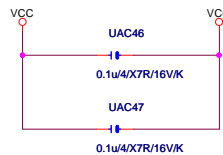
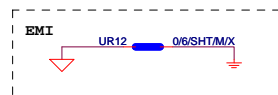
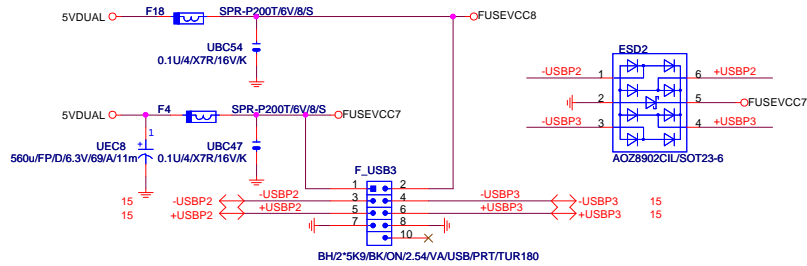
FRONT SIDE USB1



FRONT SIDE USB2

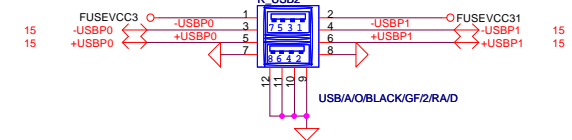
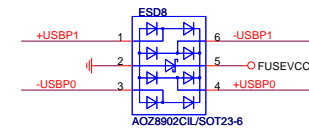
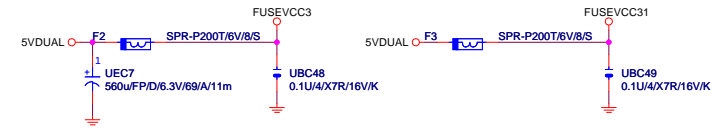
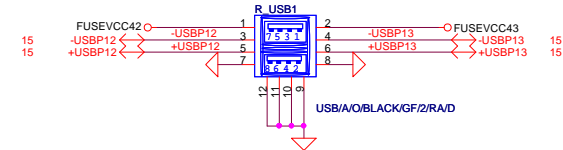
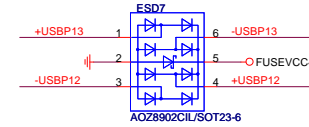
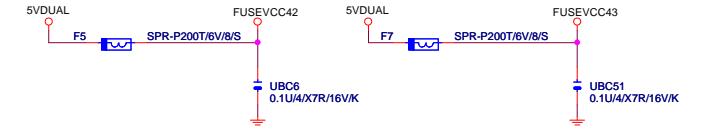


FRONT SIDE USB3



Please close 前後窗各一顆USB3.0

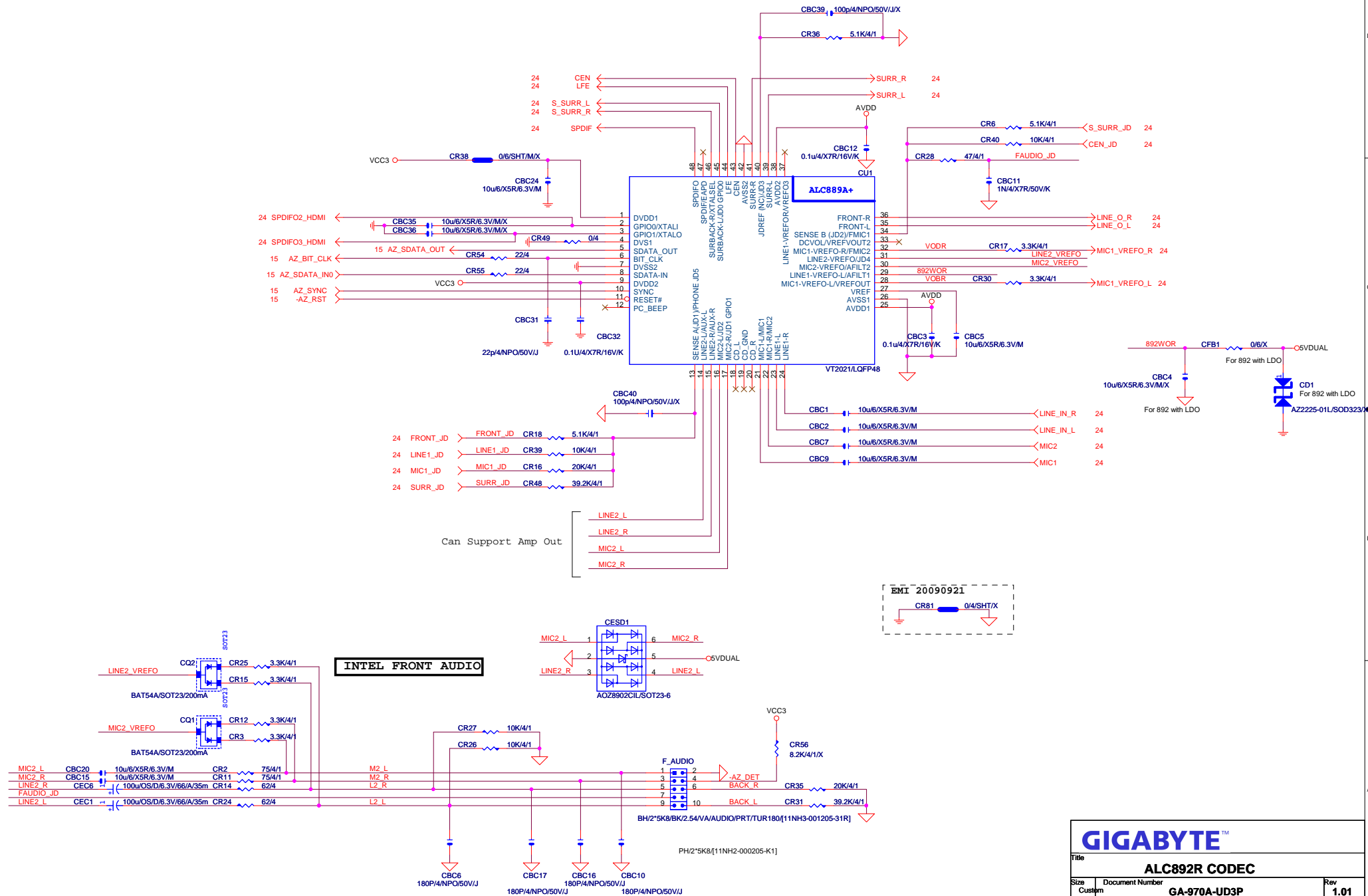
REAR USB

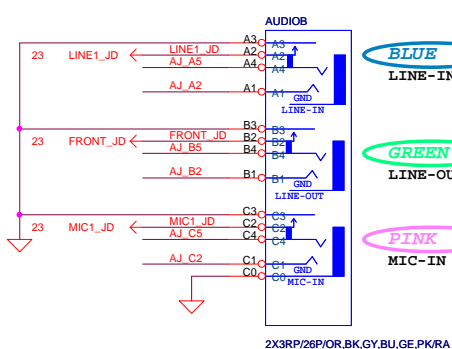
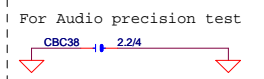
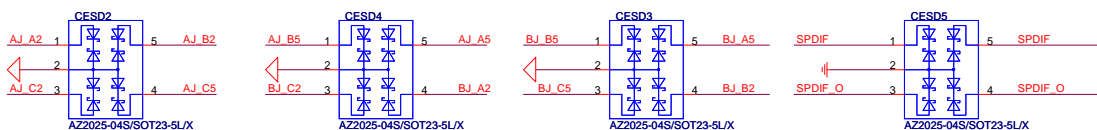
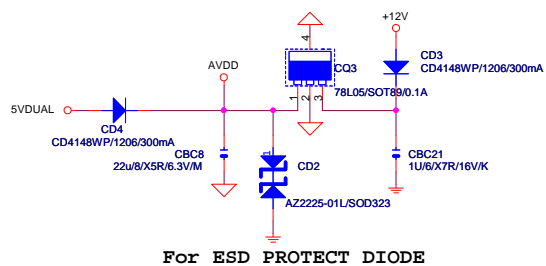
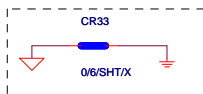


GIGABYTE

COM/LPT/F_USB/PWR

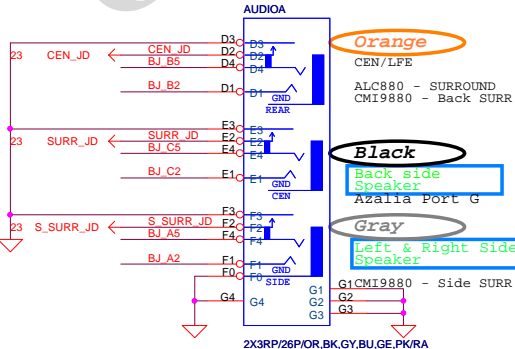
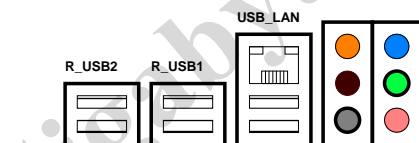
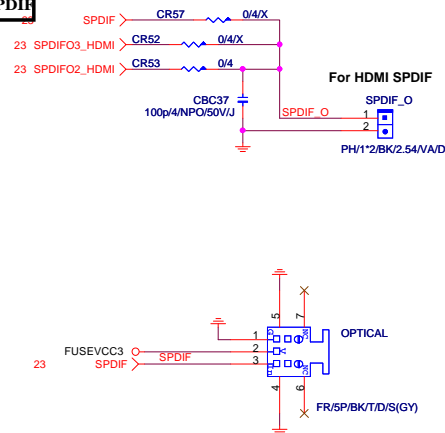
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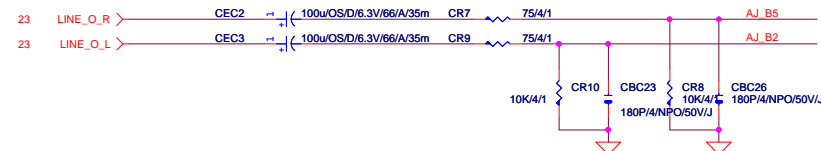
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SPDIF

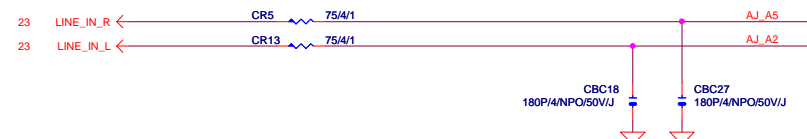


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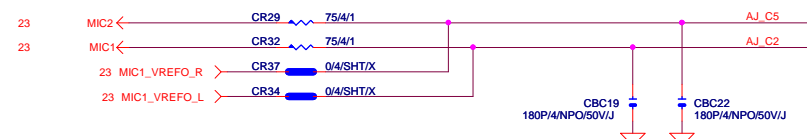
LINE OUT FRONT OUT



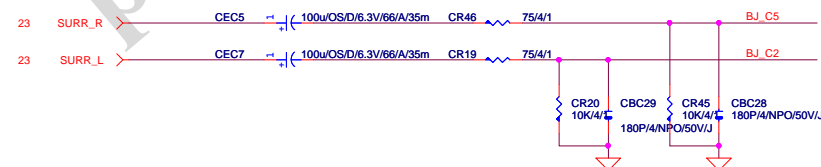
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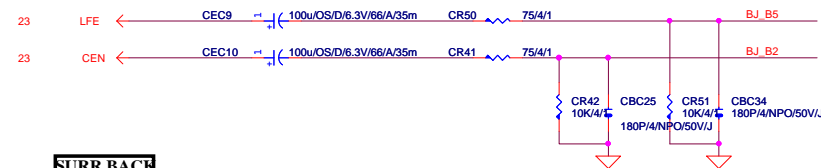
MIC



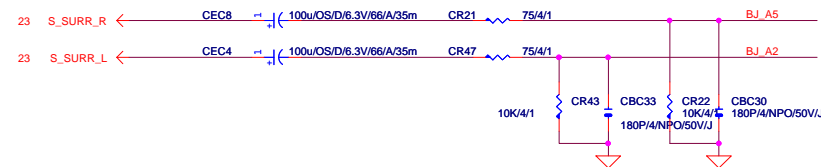
SURROUND



CEN/LFE



SURR BACK

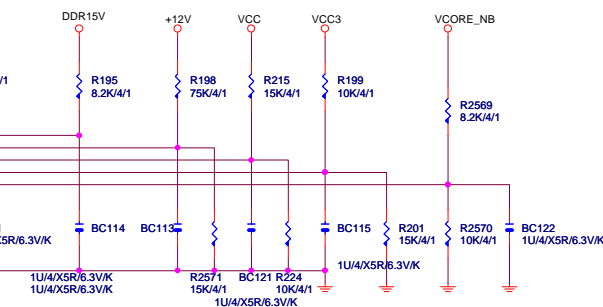
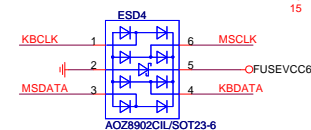
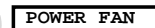
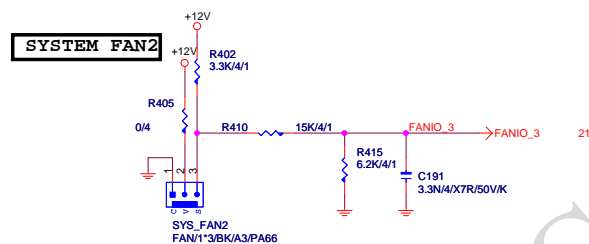
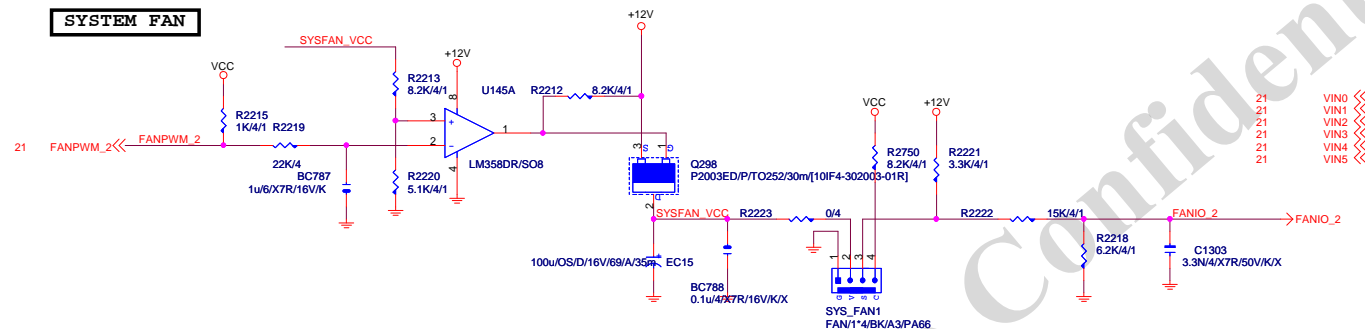
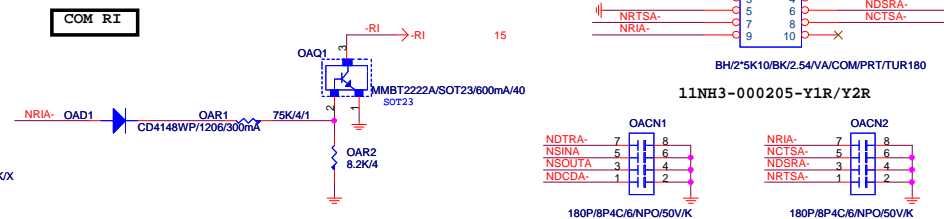
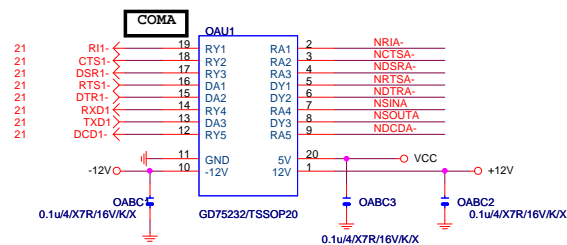
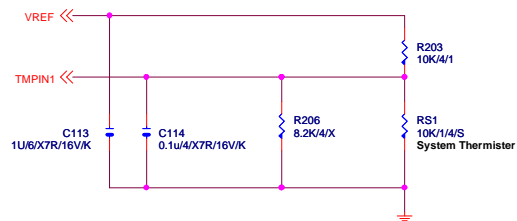


GIGABYTE

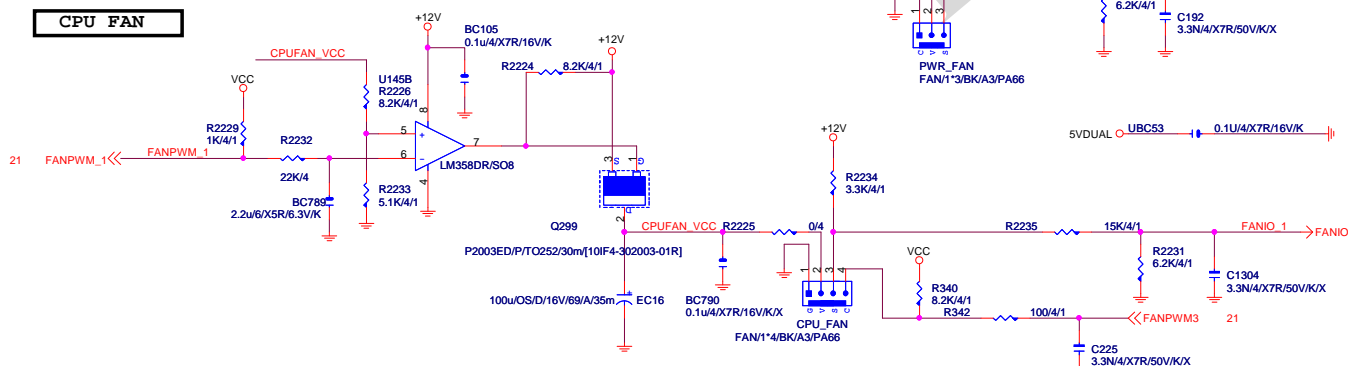
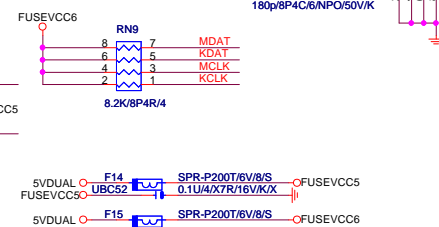
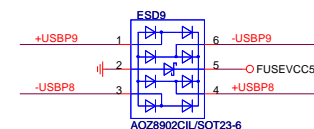
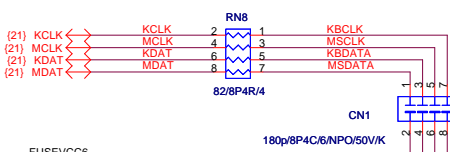
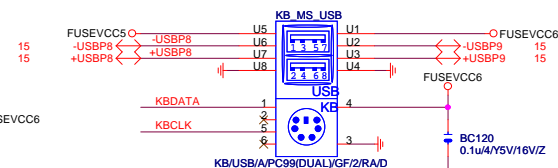
AUDIO JACK

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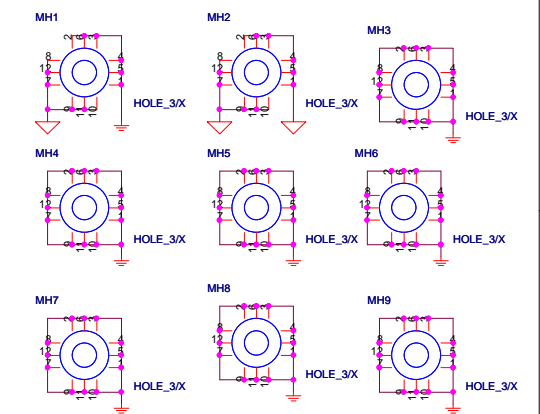
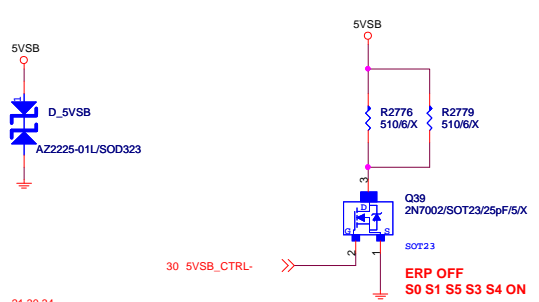
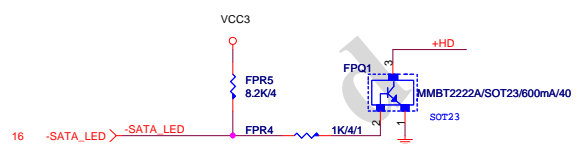
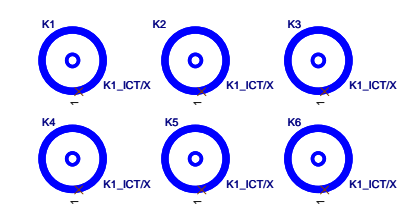
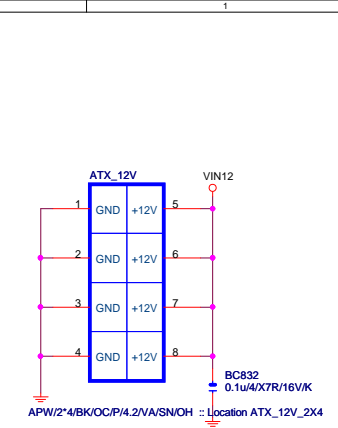
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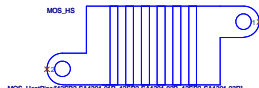


KB & USB

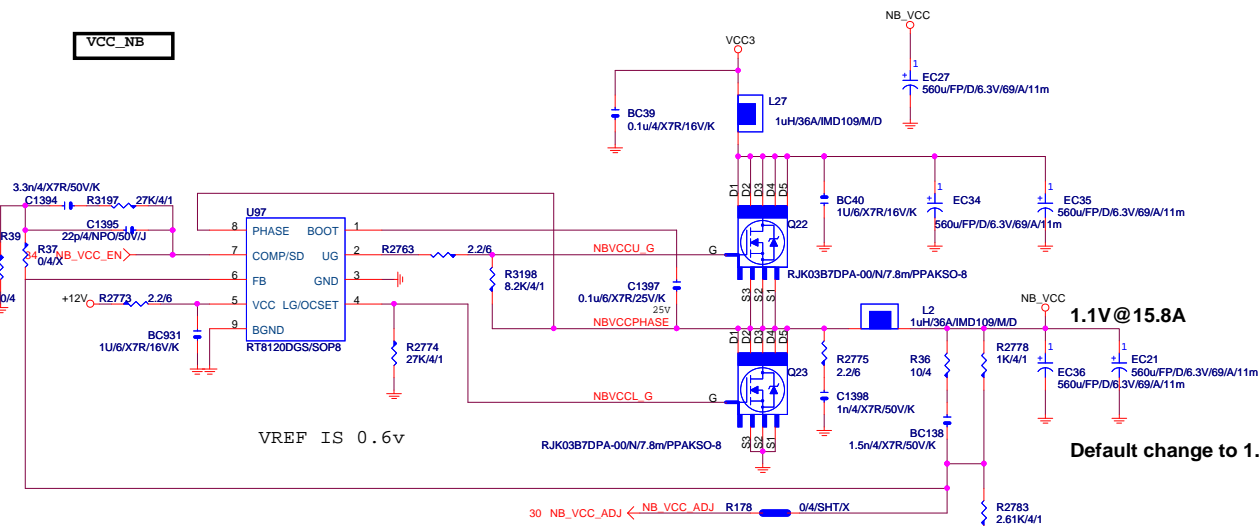


Title			
FAN/HWMO KB/MS			
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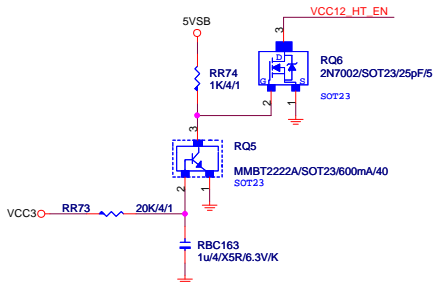




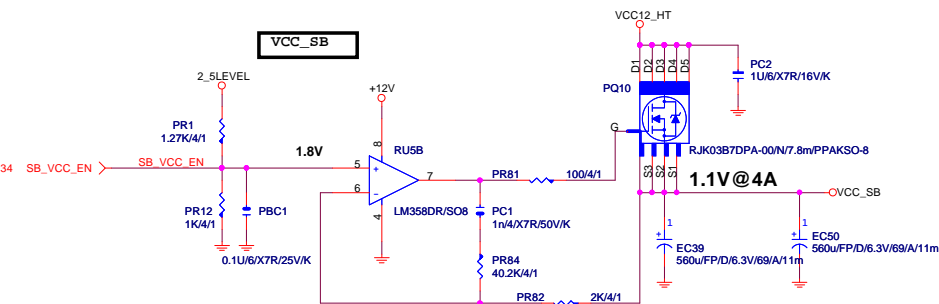
VCC_NB



Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

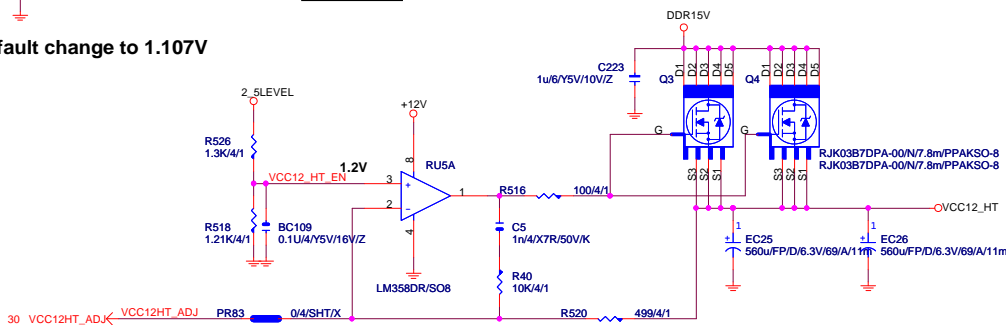


VCC_SB

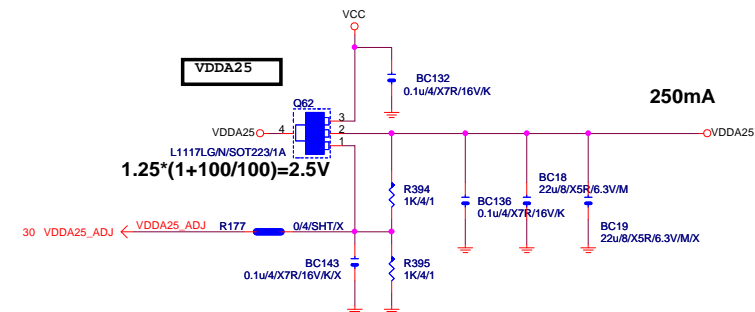


Default change to 1.107V

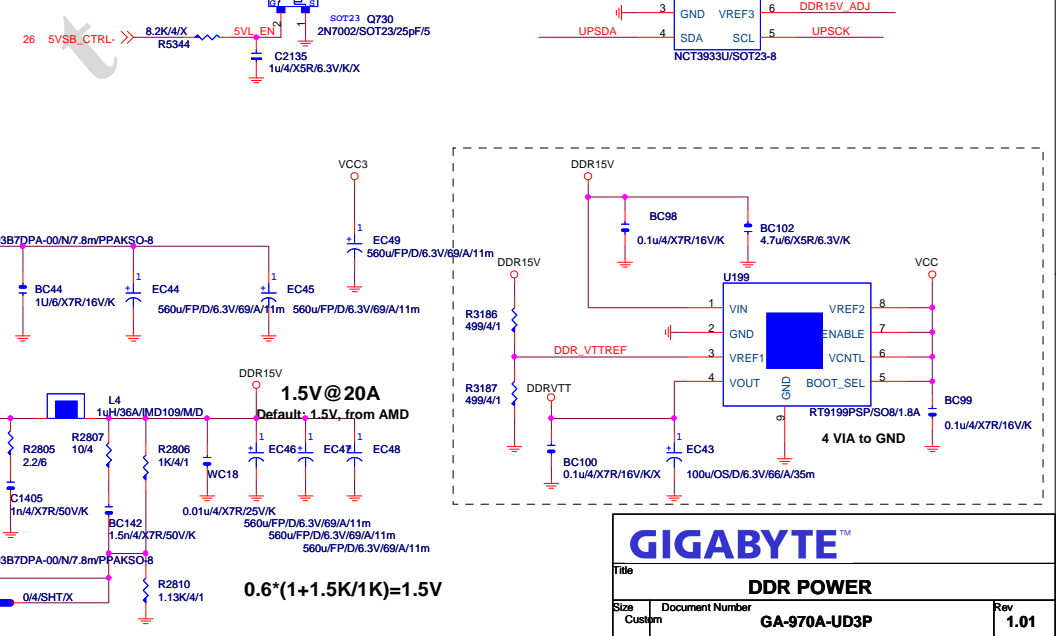
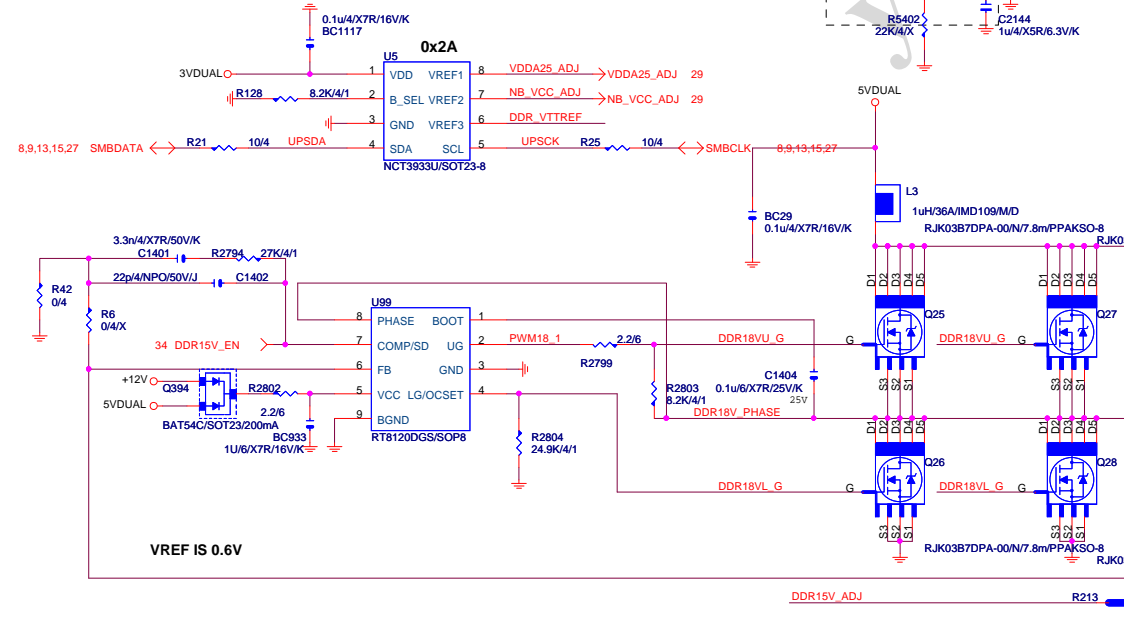
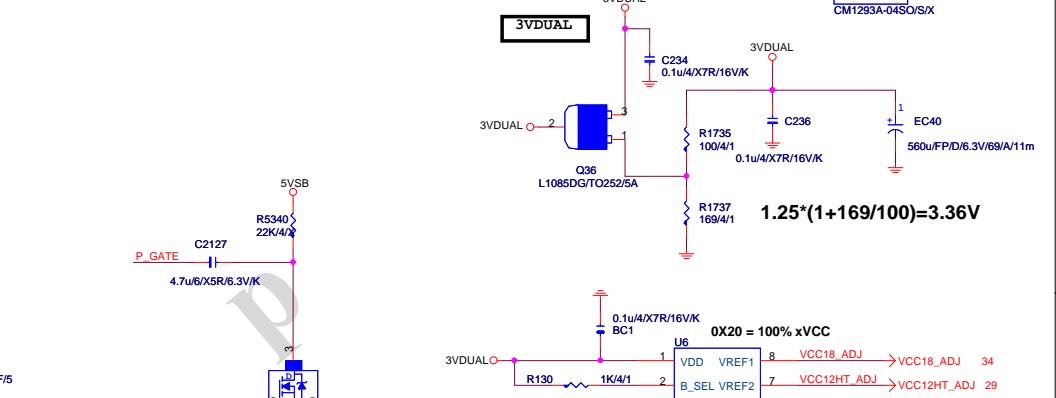
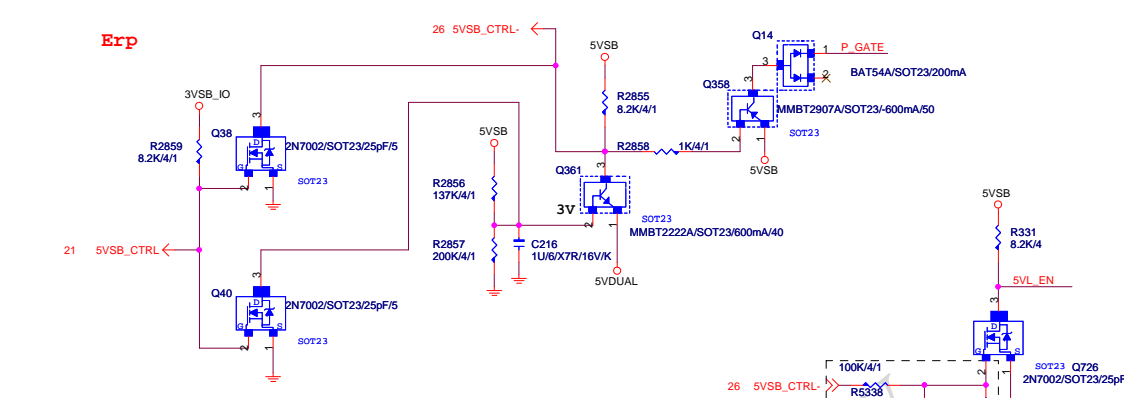
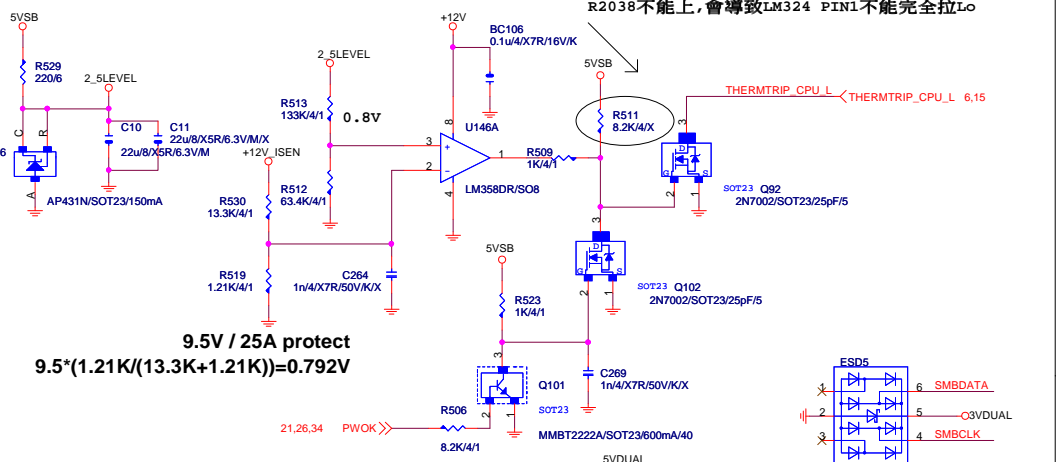
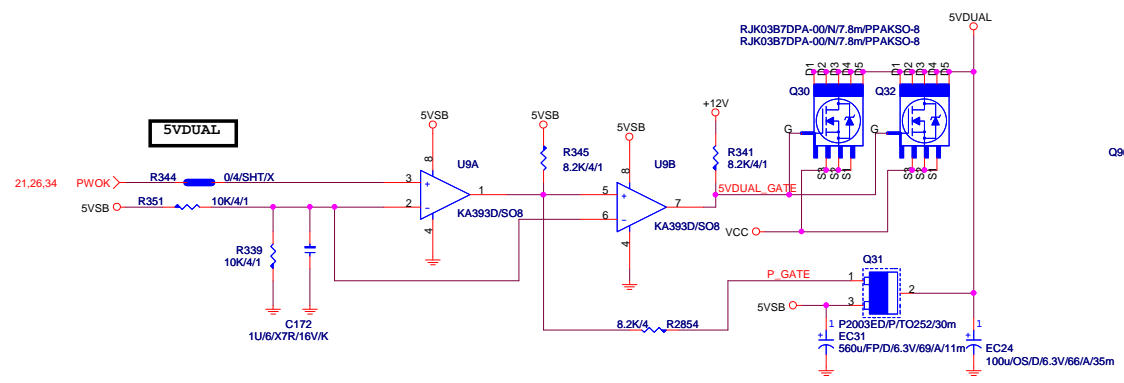
VCC12_HT



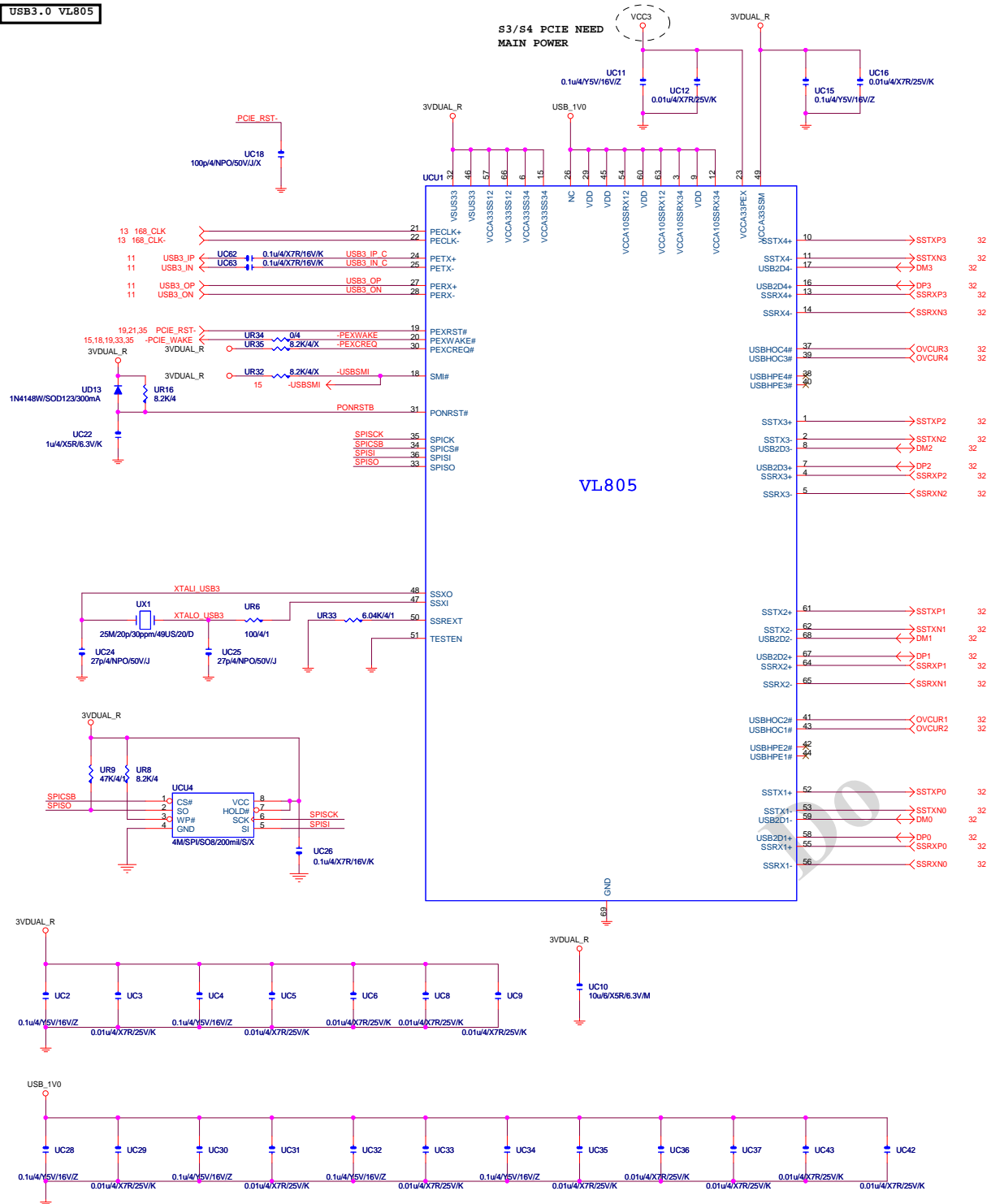
VDDA25



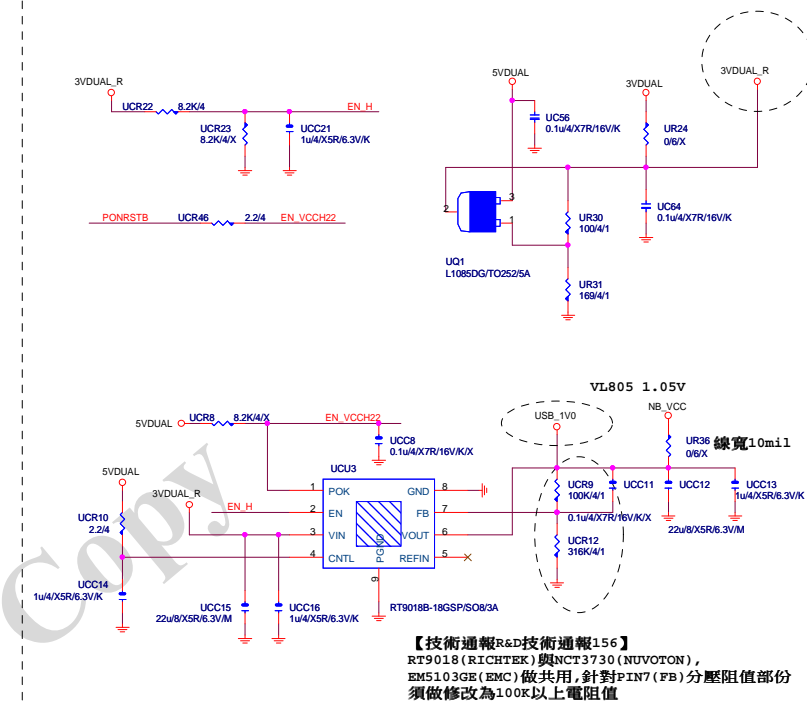
GIGABYTE™



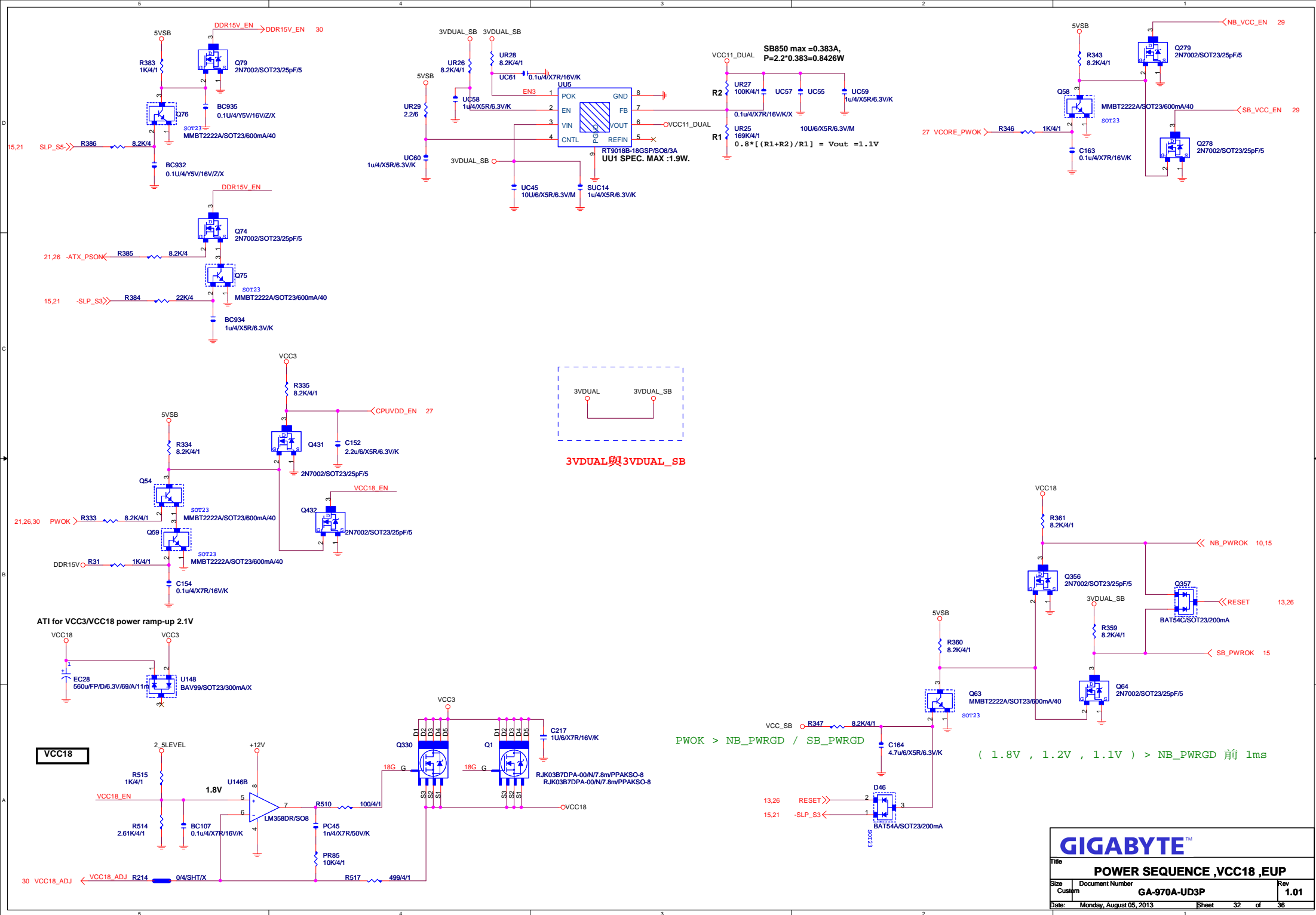
USB3.0 VL805

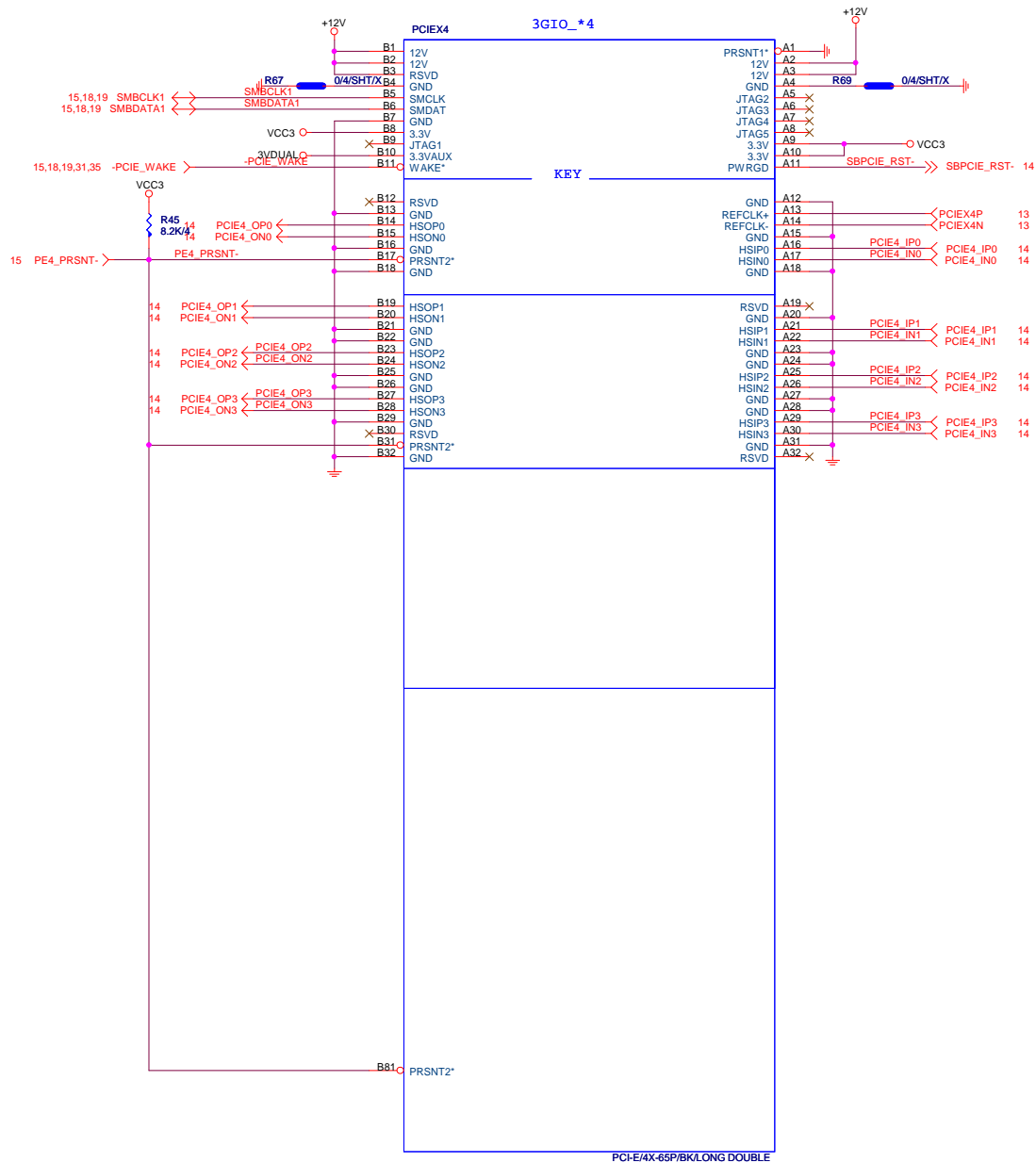


USB3.0 POWER

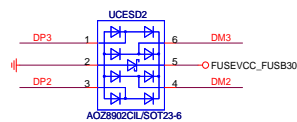
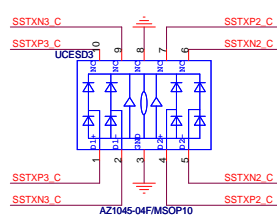
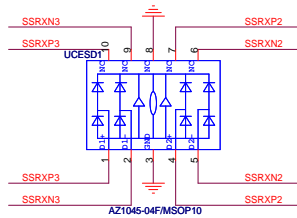
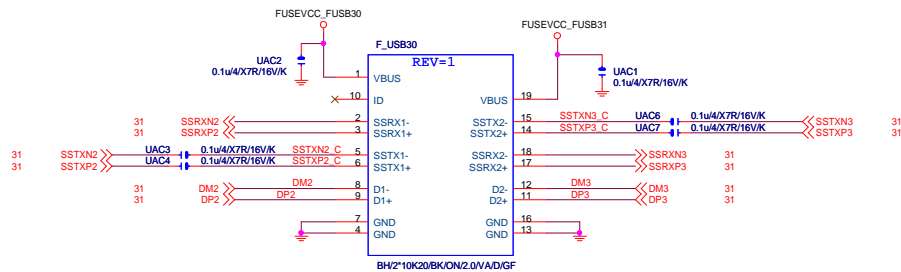


【技術通報R&D技術通報156】
RT9018(RICHTER)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
須做修改為100K以上電阻值

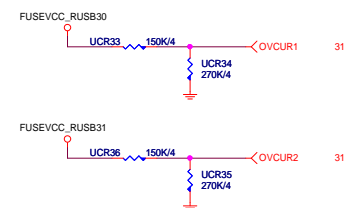
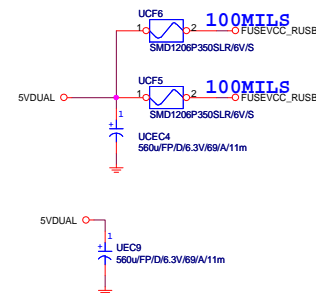
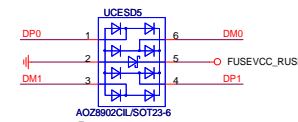
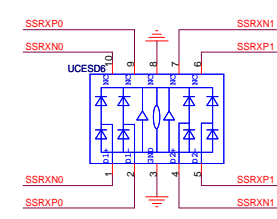
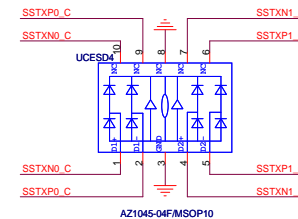
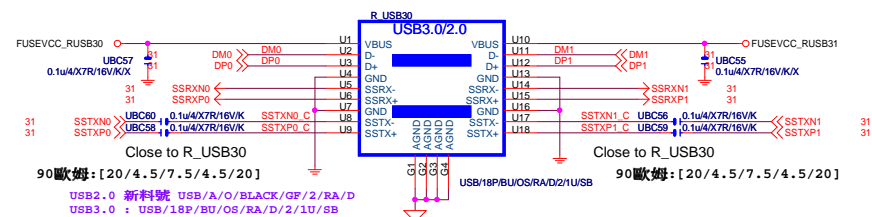




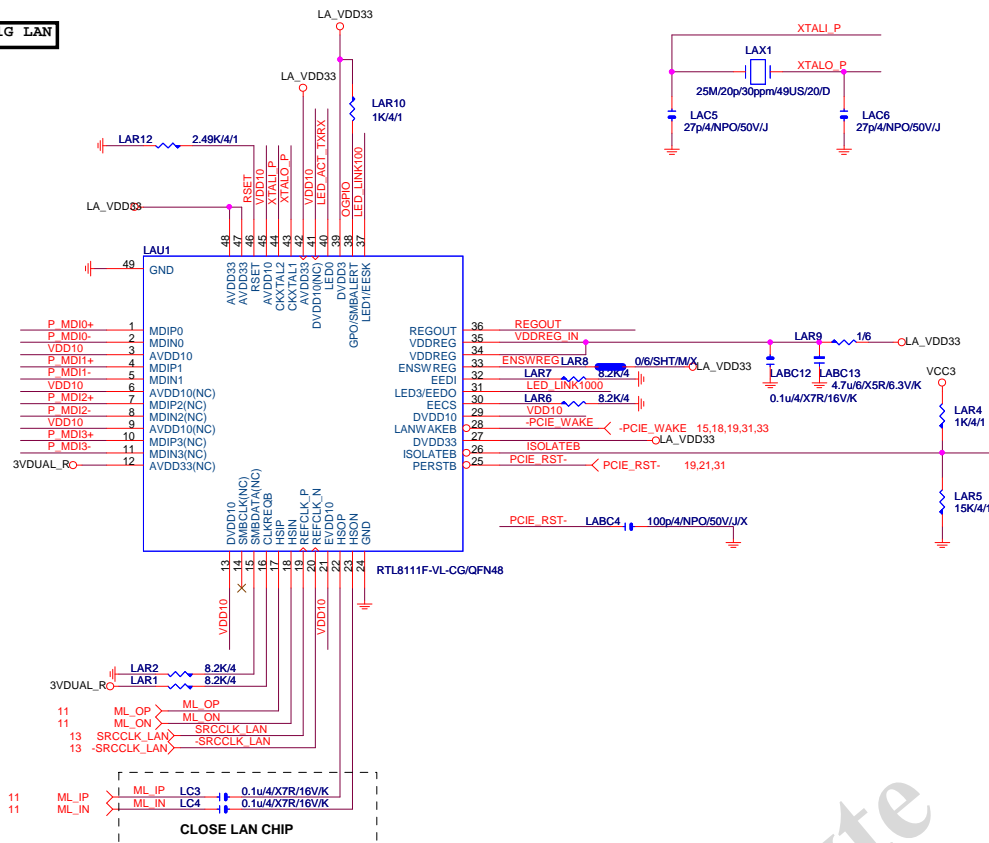
FRONT SIDE USB3



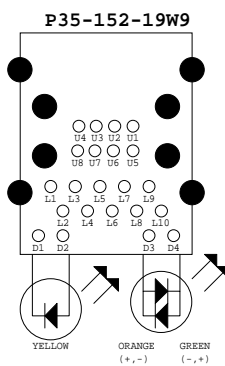
REAR SIDE USB3



PCIE-1G LAN

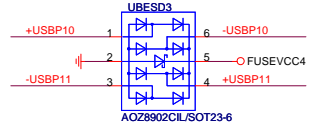
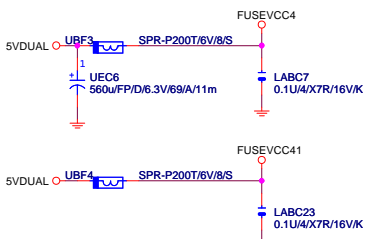
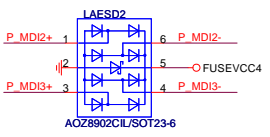
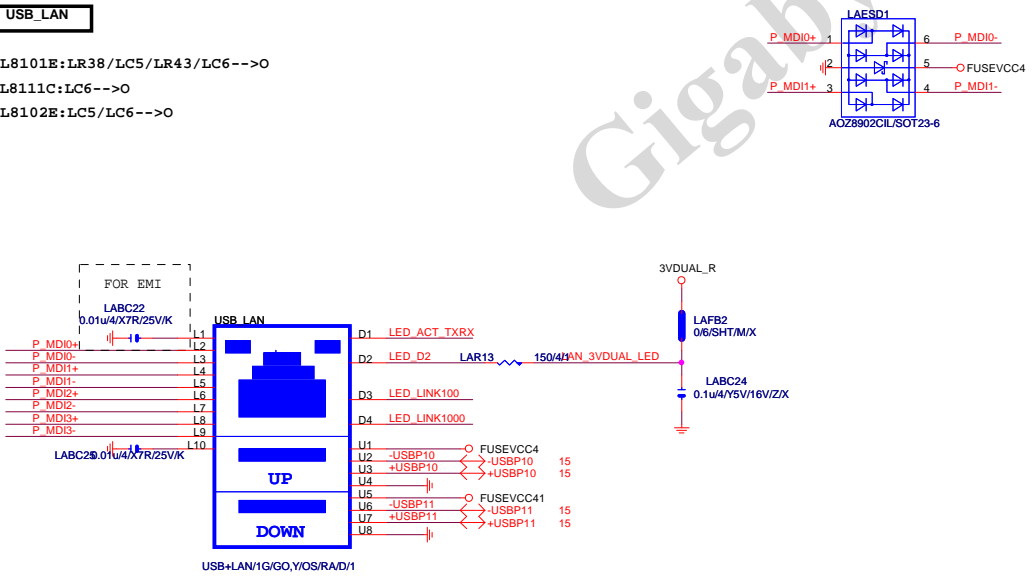


USB LAN CONNECTOR

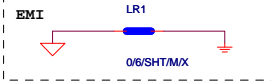


USB LAN

RTL8101E:LR38/LC5/LR43/LC6--->O
RTL8111C:LC6--->O
RTL8102E:LC5/LC6--->O



RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



GIGABYTE		
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